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Study of Operational Amplifier Test Procedure and Methods

Kumari Archana[1], Pramendra Ranjan Singh[2*]
[1]Research Scholar, Department of Physics, J. P. University, Chapra, Bihar, India
[2]Principal, Narayan College Goryakothi, Siwan, J. P. University, Chapra, Bihar, India

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ABSTRACT

In this paper, we present about the study of operational amplifier test procedure and methods. Operational Amplifiers (Op-amps) are one of the most widely used building blocks for analog and mixed-signal systems. They are employed from dc bias applications to high-speed amplifiers and filters. General purpose op-amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. The two-pole model widely used in the test analysis to assess the parameters of an op amp is not accurate and may be unsuitable for gain boosting op amp designs. A more complex model with more than two poles may require tedious analysis and a large amount of calculation. Most reported op amp measurement methods require a complicated test circuit, delicate calibration, and sophisticated test instrumentation. The practical bench test of the open loop gain along with other op amp characteristics are addressed alsoin this paper.

Keywords : High Gain Op Amp, Low Power Op Amp, Compensation Techniques.

I. INTRODUCTION

With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly. Simulation and experimental results to measure the open loop gain of the op amp can be found in [1–3]. The experimental measurements of the common mode rejection ratio and the power supply rejection ratio are proposed in [4]. But it becomes more difficult to measure the op amp characteristics, especially the open loop gain, as the power supplies decrease for lower voltage processes. When the multiplication of input referred noise and the open loop gain of the op amp [5] exceeds the voltage level of the power supplies, it is difficult to directly measure the open loop gain of the op amp. In addition, if the signal magnitude is even smaller than the noise magnitude at the input, the output waveform would have little meaning. The measurement of a real chip is more difficult than performing a computer simulation of the circuit. The environment in the real world is always full of noise and interference. Special attention is needed to make sure that the test results are valid.

The setup of the chip test and the debugging of the problems encountered during the test are now presented.

II. POWER SUPPLY CURRENT TEST AND DEBUGGING

A "functionality" test may be defined as applying an input signal to the device under test and observing the expected output. In general, the measurable parameters of the experimental design are simulated using different versions of SPICE simulators. A table of expected results could be tabulated. For example, power supply current, gain, and bandwidth for different closed loop feedback resistor ratios can be simulated, measured and compared to test results. The validity of the chip performance can then be evaluated by comparing the experimental results with the simulation results. A specific procedure needs to be done to make sure the op amp circuit is not affected by the digital circuit on the same chip since the pure analog op amp circuit is fabricated with the A/D mixed signal circuit of another researcher on one chip. Due to the lack of pins, some of the pins are even shared between the different circuits. To make sure the test results are authentic, the A/D circuit sharing the same chip with the op amp circuit has to be turned off. One way to check whether the digital circuit has been shut down is to measure the current through the power supply and compare the current to the value given by simulation. If the two elements are close to each other, the credibility of the test board is increased. The interconnection of the circuits is necessary for understanding the possible paths of the interference coming from the A/D circuit. Fig.1 shows the placement between the op amp circuit and the A/D mixed signal circuit.

In Fig. 1, gnda denotes the analog ground while gndd represents the digital ground. Vcc is the analog power supply and Vdd represents the digital power supply. It is clear that the positions where the op amp circuit connects with the A/D circuit are the analog power supply Vcc and the analog ground gnda. Because analog ground connects to the digital ground through the substrate, the op amp circuit is also associated to the A/D circuit through the substrate.

To see how the digital circuit affects the op amp circuit, a test circuit is set up to measure the power supply current. Fig. 2 is the schematic of a simple test circuit to check the possible parasitic currents. A 10 resistor is placed between the negative power supply and the negative supply terminal pin of the op amp. The pins 21 and 26 are the common analog positive supply voltage Vcc which is shared between the op amp circuit and the analog part of the mixed A/D circuit. They are tied to 1 V voltage source for the configuration of feedback op amp test.

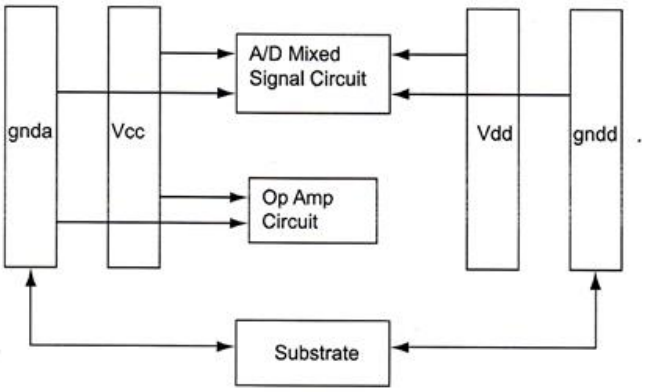

Fig. 1 : The interconnection of the chip

The pins 20 and 27 are the common analog negative supply voltage Vss (the P substrate of N channel device) shared between the op amp circuit and the analog part of the mixed A/D circuit. Vss is also called analog ground gnda in an alternative way. They are tied to -1 V source in this test circuit. The pins 6 and 40 are the digital ground of the A/D circuit. They are tied inside the chip layout to analog ground pins 20 and 27 which are used for the most negative analog supply -1 V. As a result, the analog ground is connected with the digital ground due to the common substrate in the process. The pins 1 and 15 are the digital power supply voltage Vdd of the digital part of the mixed A/D circuit. They are tied to the nwell

voltage, which changes from -1 V to 1 V during test. The current is measured by recording the voltage across the 10 resistor between the -1 V dc source and the analog negative voltage terminals pins 20 and 21. By adjusting the digital supply voltage Vdd, which is also the nwell voltage, the current through the op amp circuit power supply is shown in Table 1. The simulated current of the op amp supply by CADENCE is around 55 μA.

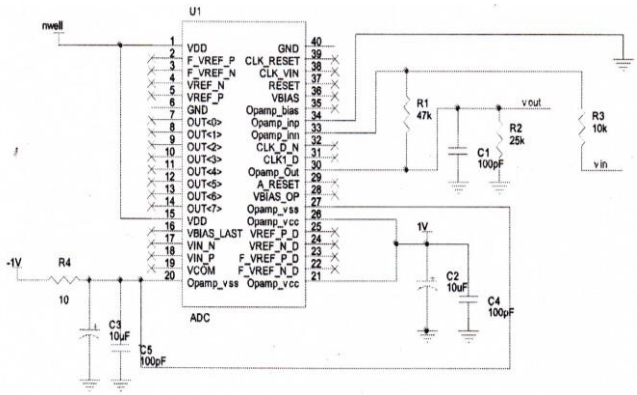

Fig. 2 : Debugging circuit setting

Table 1: The test results of the current of the op amp chip

nwell voltage (Vdd)	Current	if op amp functions
folating	200μA	no
-1 V	48 mA	no
0 V	920μ A	yes
1 V	5.99 mA	yes

When the digital power supply Vdd is floating (not connected to anything), the current flowing through the 10 resistor is under 200 μA (the lowest current recorded in the table). At that point, the op amp does not function. For example, with a 100 mV sine wave input, with the feedback inverting gain at 4.7, the output waveform does not show any gain over the input. Consequently, Vdd can not be left floating. The op amp circuit in feedback connection still does not function as an amplifier if the digital supply voltage Vdd is in the range of -1 V to -0.4 V. When Vdd gets close to - 0.3 V, the op amp circuit starts to work as a feedback amplifier with some distortion on the output waveform. The op amp circuit functions when the digital power supply Vdd is tied to the highest voltage supply 1 V as well as when Vdd is tied to the middle voltage level 0 V. When Vdd is 1 V, the current 5.99 mA is much higher than the value 920 μA measured while Vdd is set at 0 V. After careful inspection on the layout of the whole chip, it is found that the analog op amp circuit is put on the digital part of the ESD pads used to protect the integrated circuit from electrostatic damage. The left side is the analog part of the mixed A/D circuit and the right side includes the digital part of the A/D circuit and the analog op amp circuit which should not have been surrounded by the digital ESD. The analog ESD is separated from the digital side. The ESD at the left part is connected to the analog power source and the analog ground. Instead, the ESD at the right part uses the digital power source and the digital ground. Unfortunately, the op amp circuit, which is at the bottom of the chip, is put on the digital ESD side. This explains that why the op amp could not function when Vdd is floating or connected to -1 V. Since the ESD is mainly comprised of a diode connected PMOS at the top and a diode connected NMOS at the bottom as shown in Fig. 3. If Vdd is set lower than the voltage level at the pad, the PMOS will be forward biased. Even though the total current at the analog ground Vss is 5.99 mA when Vdd is tide to 1 V, most of the current might come from the digital current which is not related to the analog op amp. With the ESD circuit functions, one possible reason for this large current might come from the incomplete shut down of the A/D digital circuit. Manually turning off the digital circuit is applied to the chip under test. A sine wave with low frequency around 10 KHz is connected to the digital pin Clk_vin of the A/D circuit while Vdd is kept constant at 1 V.

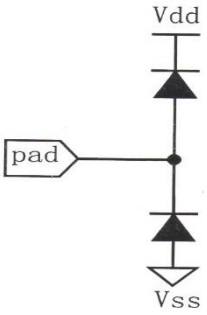

Fig. 3: ESD circuit

The current at Vss was checked and found to decrease from 5.99 mA to about 160 μA. The input signal is then disconnected from the digital pin Clk vin, the current at Vss is measured to be near 60 μA. The op amp is assumed to operate with the correct current since the measured current value is very close to the simulated value, which is 55 μA. The small difference might come from the current of the analog part of the mixed A/D circuit and the leakage current. The op amp in feedback connection is then tested and the performance is as expected. One important lesson learned here is not to put the sensitive analog circuit close to the power digital device.

III. OP AMP TEST SETUP

A simple test circuit can be built by placing components on a breadboard and connecting them with jumper wires. It is convenient to get a rough estimation of the chip performance on a breadboard in a short period of time. It also saves money since the breadboard is a cheap reusable solderless device. But the noise contribution from the breadboard and wires is usually high enough to affect the behavior of the circuit experiments. The specific printed circuit board (PCB) is necessary for testing circuit designs, especially for low voltage high gain op amps which demand low noise environment. The layout of the PCB designed for the op amp chip test is shown in Fig. 4.

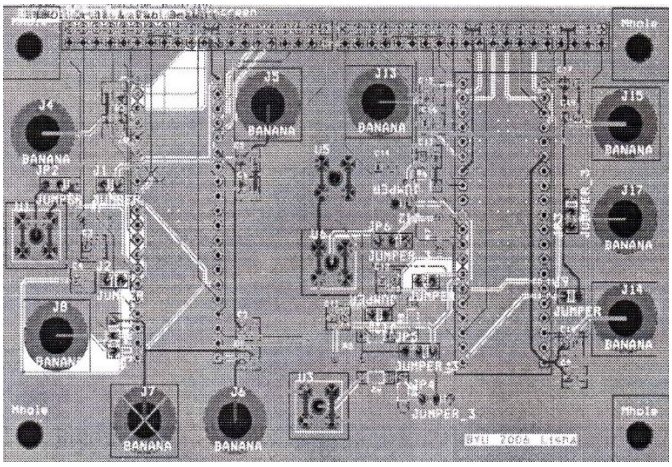

Fig. 4 : The PCB layout

Two different settings are provided on the PCB. The one on the left is the configuration set up for testing the unit feedback response. The one on the right can provide various feedback gains to measure the gain and bandwidth for the corre- sponding feedback factor F. Decoupling capacitors are used to reduce the fluctuation noise from the source supplies.

IV. OP AMP CLOSED LOOP CHARACTERISTIC TEST CONFIGURATION

The configuration for measuring the unit feedback response, the slew rate, the settling time, the input common-mode voltage range, and the input-offset voltage is shown is Fig. 5. The input offset voltage is not only due to the small bias mismatches in design but mostly caused by device and component mismatches through fabrication. Most simulators are not capable of predicting device and component mismatches from the fabrication process.

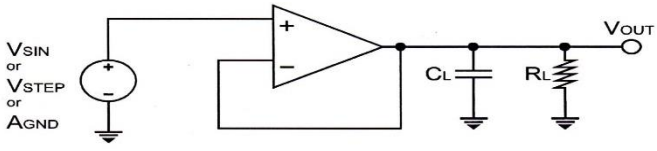

Fig. 5 : Op amp unit feedback configuration

The input offset voltage is simulated to be only 37 nV by CA- DENCE spectre. For over 10 chips tested, the

input offset voltages range from 0.3 mV to 3 mV due to the process variation. The configuration for measuring the gain bandwidth and output voltage swing is shown in Fig. 6. The value of the resistor Rf should be large enough compared to the load resistor RL in order not to cause significant dc current load on the output of the op amp.

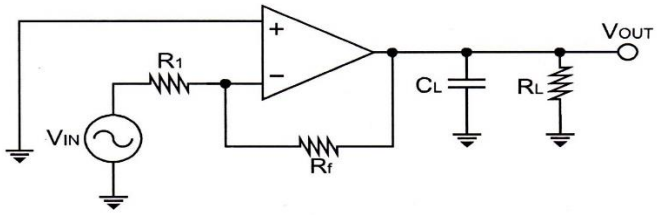

Fig. 6 : Op amp gain bandwidth configuration

V. OPAMP OPEN LOOP GAIN TEST METHODS

While the closed loop properties can be easily and straightforward to test with feedback setting, measuring the open loop characteristics is much more difficult to perform. The differential gain of an op amp is quite high. A small offset voltage is generally enough to saturate the op amp to the power supply level. With the supply voltages decreasing, even a very little input noise can drive the op amp out of the power supply limits. For the composite cascode op amp with a gain of one million at ± 1 power supplies, an input noise level as low as 1 μV is sufficient to saturate the op amp. It is hard to directly measure the open loop gain of the op amp. Suitable approaches are needed to measure the open loop gain for low voltage high gain op amp.

One conventional way to check the open loop frequency response is by measuring closed loop gain phase response at various values of feedback factor F. If the measured closed loop gain phase response at different values of F could match the simulated closed loop gain phase response respectively, there is a good chance that the open loop gain phase response of the op amp under test is similar to the simulated open loop gain phase response. There might be some difference between the simulated closed loop response and the measured closed loop response due to parasitic effects and process variations. The dominant pole of the composite cascode op amp under test is only a couple of Hz after compensation by simulation. A second order op amp model can be built, if the equivalent second pole, which patterns all non-dominant higher poles into a single pole, can be found. Then, the closed loop transfer function becomes

$$G_d(s) = \frac{\frac{A_0}{1+A_0F}}{1+\frac{\frac{s^2}{P_1P_2}+s\left(\frac{1}{P_1}+\frac{1}{P_2}\right)}{1+A_0F}} \qquad (1)$$

The corresponding expressions of the gain and phase of the closed loop transfer function are denoted as

$$G_{dB}(\omega) = 20\log\left|\frac{A_0}{1+A_0F}\right| - 20\log\left|1-\frac{\frac{\omega^2}{P_1P_2}}{1+A_0F}+ j\omega\frac{\left(\frac{1}{P_1}+\frac{1}{P_2}\right)}{1+A_0F}\right| \qquad (2)$$

and

$$G_{phase}(\omega) = \arctan\frac{\frac{\omega\left(\frac{1}{P_1}+\frac{1}{P_2}\right)}{1+A_0F}}{1-\frac{\frac{\omega^2}{P_1P_2}}{1+A_0F}} \qquad (3)$$

It is possible to predict the poles and the midband gain by using the experimental gain and phase of the op amp measured at different values of F. With a gain phase meter, the closed loop response can be tested and compared to the simulated response. This indirect way by employing a two-pole op amp model to estimate the characteristics of the op amp is similar to the studies reported in [6-8]. Those reported measurement approaches do not fully consider the nonlinear distortion or more complete models with orders higher than two to represent the op amp behaviour accurately. The two-pole model works well for op amps with one low dominant pole and a second pole higher or near the unity frequency. For op amps using cascade connections or other kinds of gain boosting schemes, the second pole of the op amp will be much lower than the unity frequency. Moreover, many multistage op amps have zeros and some significant poles besides the second pole. The classical

two pole model assumption does not hold for these op amps and is not capable of providing precise modeling and measurements.

In [9], more complicated models of op amps are considered and the calibration of the measurement setup [10] are presented. Most methods require a lengthy procedure of calculations, sophisticated instrumentation, and/or complicated bench setup to implement the test. In addition, most methods do not work well for CMOS devices with low power supply voltage.

To address the inaccuracy of applying the indirect modeling of feedback op amps to describe the open loop characteristics, other simple but reliable test methods of op amps using typically available bench test equipment are investigated and presented. The supplies of 1 V and -1 V are applied to the op amp chip. The power consumption of the chip is around 120 μW based on the supply current which is measured to be close to 60 μA. The offset voltages on a sample of ten chips was found to be between 0.3 mV and 3 mV. The output load of the op amp consists of a 100 pF capacitor in parallel with a 25 k resistor. The CMRR and PSRR are measured to be above 100 dB. The main test results are summarized in Table 2.

Table 2: Opamp Test Results

DC Gain (dB)	≥117
GBW(MHz)	1.2
PM(^{0})	43
SR^+/SR^-(V/μs)	0.27/0.43
Ts^+/Ts^-(μs) (to1%)	3.85/2.2
Power μW)	≤120
Supply Voltage (V)	±1

The lack of high precision signal generator that can produce low frequency signal with little distortion prevents the more accurate evaluation of the open loop gain. A spectrum analyzer plot shows the signal generator available in the analog lab produces a low frequency signal with significant harmonic distortion. Strategy three estimates the op amp gain to be above 100 dB. However, the more precise measurement of the gain is not possible due to the noise of the test chip, which is presented as the fluctuation of the amplified offset voltage. The result of 117 dB open loop gain is given by strategy four because the measurement of the slope instead of the magnitude value is more robust to noise. Using a voltage divider to decrease the input signal to get an exact measurement of the open loop gain will eventually be limited by the input noise floor of the test chip. The extremely low signal noise ratio leads to the corruption of the output signal slope. The further evaluation of the op amp open loop gain as the expected 120 dB is prohibited by the considerable flicker noise of the MOSFET device. Nevertheless, the adequately close match between the op amp chip experimental results and the CADENCE Spectre Spice Simulation demonstrates that the prototype chip has achieved the expected performance in the case of low current weak inversion operation of the composite cascode output device.

VI. CONCLUSION

Detailed test set up, debugging, and test methods implemented to describe the op amp performance are presented in this paper. It discusses the increasing challenge to measure the high gain op amp characteristics when the power supplies are getting smaller. Several simple bench test methods are investigated and proposed to characterize the op amp characteristics, in particular the open loop gain. Those practical techniques do not require sophisticated instrumentation or a complicated lab setup. The requirements and the suitability of the different measurements in various situations are also evaluated.

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