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Area Efficient BCD Seven Segment Circuit Designing Using QCA

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ABSTRACT

Quantum-dot Cellular Automata (QCA) is a new Nano-scale technology that due to making significant improvements in the design of electronic circuits can be considered as an appropriate alternative to CMOS technology. It is an alternative nanotechnology which keeps scaling down the technology further. It can do scaling beyond to a level where complementary metal oxide semiconductor (CMOS) scaling rises the issue. QCA is seen as an emerging solution for Nano-architectures. In our work, Seven Segment Display is proposed using different gates and majority voter gate in QCA which is having less area and high performance. This nanotechnology uses different logic devices for digital circuit designing for obtaining a high rate of performance at output. This new nanotechnology uses a specific method to represent and decode the data. The main aim behind our work is to understand the basic QCA technology and to get familiar with the QCA designer software for getting involved in advanced designing of digital circuits using QCA. A seven Segment Display uses Light Emitting Diodes to display output that can be in the form of image, text or decimal number. The simulation results verify that our work is significant.

Keywords: Quantum-dot Cellular Automata (QCA), seven segment display, Arithmetic Logic Unit (ALU), Multiplexer, Full adder.

I. INTRODUCTION

QCA (Quantum-dot Cellular Automata) is one of the most attractive alternatives for CMOS technology. QCA uses the paired order of quantum dots to implement the Boolean logic functions. QCA is physical implementation of a classic cellular automata from mechanic quantum effect.

The common digital technologies use the voltage or current ranges for showing the logic values, whilst in QCA technology, the situation of electrons in quantum dots shows the binary values.

The advantages of this technology include:

1. High operational speed (Tera Hertz range),
2. Low power consumption (approximately 100),
3. High device density.

Minimum feature in CMOS has reduced after several decades, however, facing some limitation. This subject caused the rapid development of molecular plans in Nano-scale. QCA is a hopeful sample in nanotechnology, suggested by Lent et al. and created in 1997.

According to the considerable features of QCA such as high density, low power consumption, high speed function potential and pipeline being advantage, QCA is changed as an interesting alternative technology for CMOS technology.

QCA is based upon encoding of binary information in the charge configuration within Quantum-dot cells. Computational power is provided by the Columbic interaction between QCA cells. No current flows between cells and no power or information is delivered to internal cells. The interconnection between QCA cells is provided by cell-to-cell interaction due to the rearrangement of electron positions .The two electrons are loaded in antipodal sides in Quantum-dots of a QCA cell.

A standard QCA cell is constituted of four quantum dots at four corners of a square cell. In this cell, four quantum dots have been paired together by the tunnel barriers. Two electrons existing in each cell may tunnel between the quantum dots inside the cell.

The high intercellular potential barriers ensure that no electron tunnels between QCA cells. Figure shows a standard QCA cell with four quantum dots located at its corners.

The efficacy of columbic interaction have run two electrons each to the cell diameters. The polarization of both stable states in cell diameters provides binary logic 0 and binary logic 1.

Figure exhibits the state of electrons placed in cell diameters and 0 and 1 binary information. If two cells are located next to each other, the columbic interaction between the electrons causes the cells to have equal polarization and the same value of its left side cell. In Fig. some of QCA cells have been located beside each other and formed a wire in QCA. In QCA technique, the wires are 45 and 90 degrees. Both wire types are used in the cross over and arrays intensively.

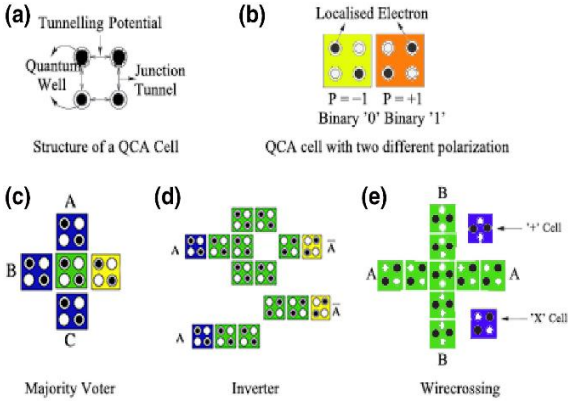

Fig. 1 a) QCA cell b) QCA Polarization c) Majority Voter d) Inverter e) Wire crossing

QCA clocking has been performed through timing in four distinct phases and required for both combinational and sequential circuits. Clocking not only controls the data current but provides the actual power in QCA circuits. The clock used in QCA consists of 4 phases: Switch, Hold, Release and Relax.

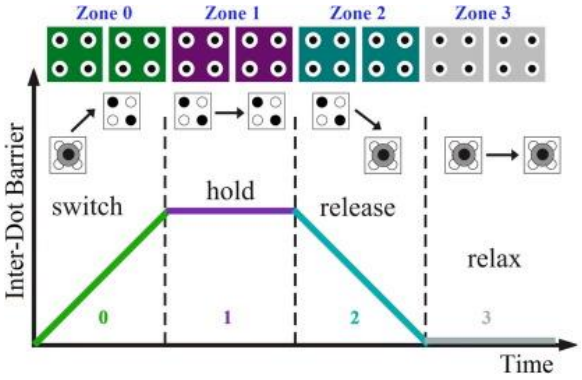

Fig. 2 QCA Clock Schemes

The signal energy lost by the medium is recovered by a new clocking. In QCA, clocking signals have been generated by an electrical field so that to control tunnel barriers in the quantum dots inside a QCA cell.

Quantum-dot cells are key components of QCA technologies to implement as Logic Gates, Wires, and Memories. The basic logic elements in QCA technology are the Majority gate and Inverter. Wires can be used for signal propagation in QCA circuits.

Logic elements such as AND gate & OR gate can be obtained by manipulating the Majority gate.

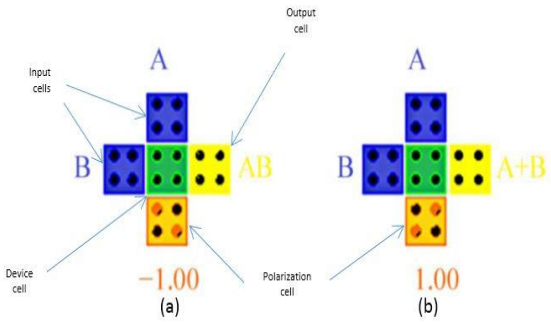

Fig. 3 AND & OR Gate

Though the technology is different from convention CMOS designs, it is effective and realistic to implement the low power logic circuits. Thus, QCA is a new innovation at Nano-scale and an appealing substitute to ordinary CMOS. It is a possible technology for the next generation of digital circuits and systems and widely utilized as a part of advanced frameworks.

II. EARLIER WORK

In the existing design BCD 7-segment display is implemented using QCA technology. Here there are four steps namely analysis, truth table design, **K-map** and designing a combinational logic circuit using QCA cells.

This display can be constructed with seven LEDs in the form of H. A truth table of this circuit can be designed by the inputs combinations for every decimal digit. For instance, decimal number '1' would control a blend of b & c.

Fig. 4 Truth Table of BCD 7-Segment Decoder

The second step is the truth table design by listing the display input signals-7, equivalent four-digit binary numbers as well as decimal number.

The tabular form of a BCD to 7-segment decoder display is shown below. The truth table consists of seven o/p columns equivalent to each of the seven segments. For example, the column for a-segment illustrates the various arrangements for which it is to be light up. Thus 'a'- segment is energetic for the digits like 0, 2, 3, 5, 6, 7, 8 & 9.

The outputs of the BCD decoder are obtained by the simplification of the min terms using K-maps.

For output P: The Boolean expression is P = A + C + BD + B'D'

For output Q: The Boolean expression is Q = A + B' + CD + C'D'

For output R: The Boolean expression is R = C' + B + D

For output S: The Boolean expression is S = A + CD' + B'D' + B'C +BC'D

For output T: The Boolean expression is T = CD' + B'D' or T = D'(C+B')

For output U: The Boolean expression is U = A + BC' + BD' + C'D' or U = A + B (C' + D') + C'D'

For output V: The Boolean expression is V = A + CD' + BC' + B'C

For output P: Figure 5 shows the designing of output P in QCA technology. It is designed by using AND, OR and NOT gates. Clock 0 and clock 1 are used in the designing.

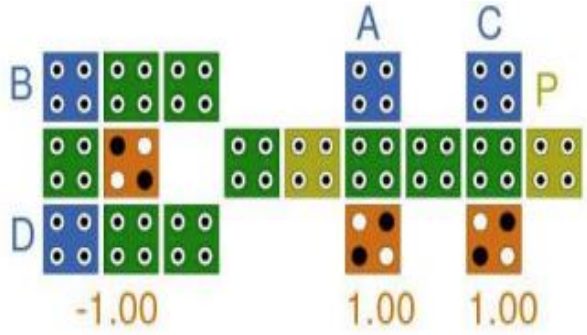

Fig. 5 QCA layout for the output P

For output Q: Figure 6 shows the designing of output Q in QCA technology. It is designed by using OR, XNOR and NOT gates. Clock 0, 1 and 2 are used in the designing. A, B, C and D are the

Digit	A	B	C	D	P	Q	R	S	T	U	V
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

inputs whereas Q is the desired output.

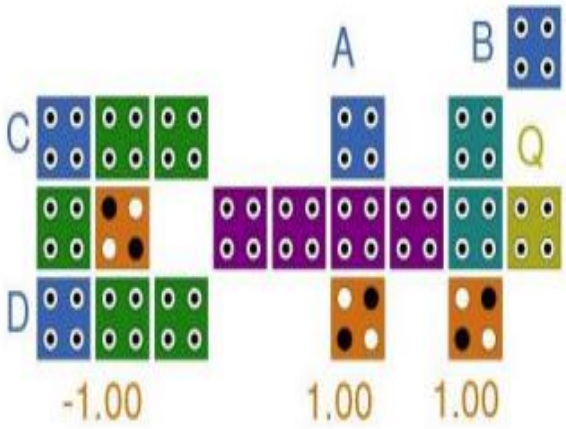

Fig. 6 QCA layout for the output Q

For the output R: Figure 7 shows the designing of output R in QCA technology. It is designed by using OR and NOT gates. Clock 0 and 1 are used in the designing. B, C and D are the inputs whereas R is the desired output.

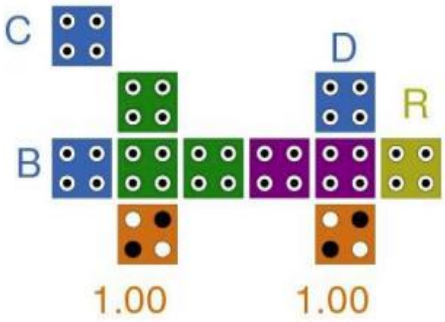

Fig. 7 QCA layout for the output R

For the output S: Figure 8 shows the designing of output S in QCA technology. It is designed by using OR, AND and NOT gates. Clock 0, 1, 2 and 3 are used in the designing. A, B, C and D are the inputs whereas Q is the desired output.

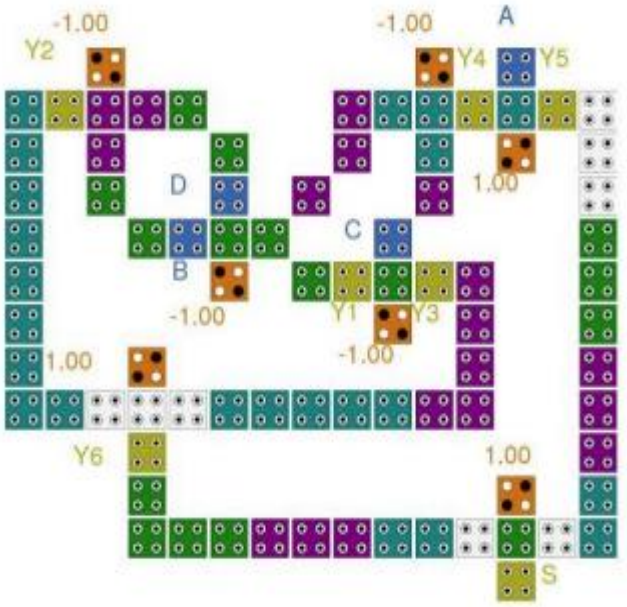

Fig. 8 QCA layout for the output S

For the output T: Figure 9 shows the designing of the output T in QCA technology. It is designed by using AND, OR and NOT gates. Clock 0 and 1 are used in the designing. B, C and D are the inputs whereas T is the desired output.

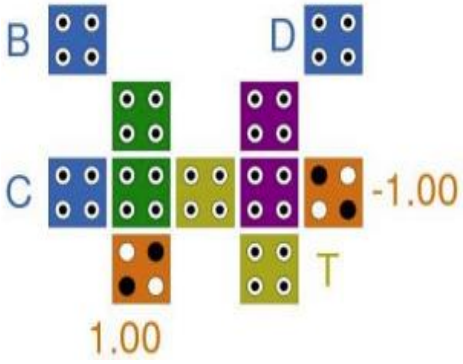

Fig. 9 QCA layout for the output T

For the output U: Figure 10 shows the designing of output U in QCA technology. It is designed by using OR and NNI gate. Clock 0 is used in the designing. A, B, C and D are the inputs whereas U is the desired output.

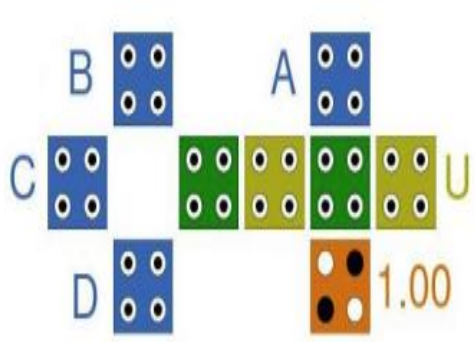

Fig. 10 QCA layout for the output U

For the output V: Figure 11 shows the designing of output V in QCA technology. It is designed by using OR and XOR gates. Clock 0, 1 and 2 are used in the designing. A, B, C and D are the inputs whereas V is the desired output.

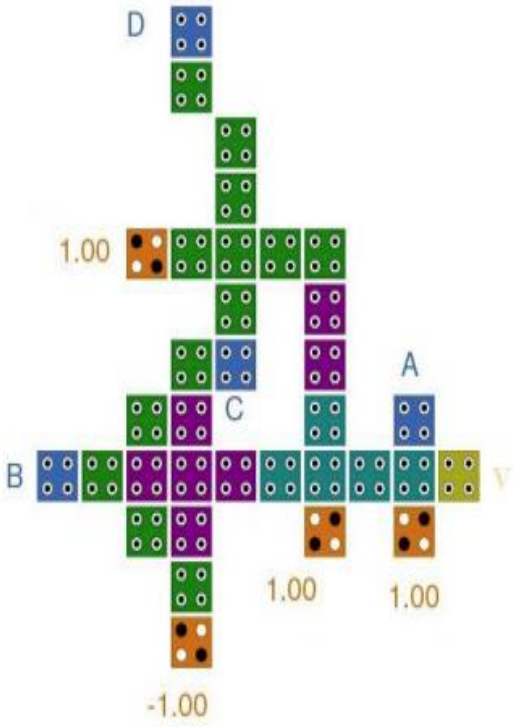

Fig. 11 QCA layout for the output V

III. PROPOSED WORK

In the proposed design a BCD to 7-segment display is implemented using QCA technology. Because of BCD i.e. from 0-9 there are three inputs X, Y&Z. The 7-segment display having total 7 lines so that the decoder outputs are a, b, c, d, e, f& g.

For output P: Figure 13 shows the designing of output P in QCA technology. It is designed by using AND, OR and NOT gates. Clock 0 and clock 1 are used in the designing.

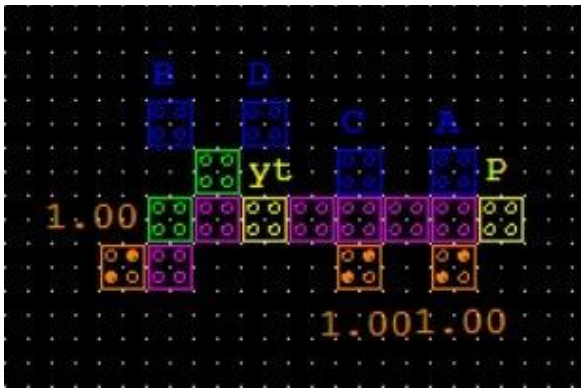

Fig. 13 QCA layout for the output P

For output Q: Figure 14 shows the designing of output Q in QCA technology. It is designed by using OR, XNOR and NOT gates. Clock 0, 1 and 2 are used in the designing. A, B, C and D are the inputs whereas Q is the desired output.

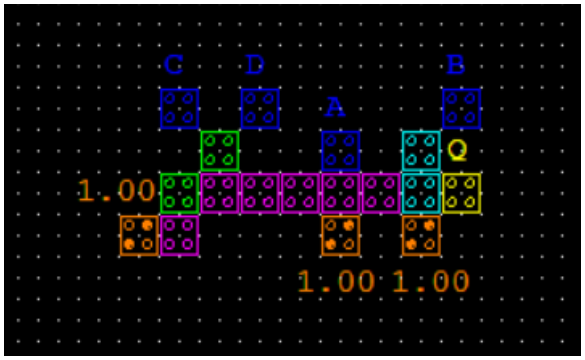

Fig. 14 QCA layout for the output Q

For the output R: Figure 15 shows the designing of output R in QCA technology. It is designed by using OR and NOT gates. Clock 0 and 1 are used in the designing. B, C and D are the inputs whereas R is the desired output.

Fig. 15 QCA layout for the output R

For the output S: Figure 16 shows the designing of output S in QCA technology. It is designed by using OR, AND and NOT gates. Clock 0, 1, 2 and 3 are used in the designing. A, B, C and D are the inputs whereas Q is the desired output.

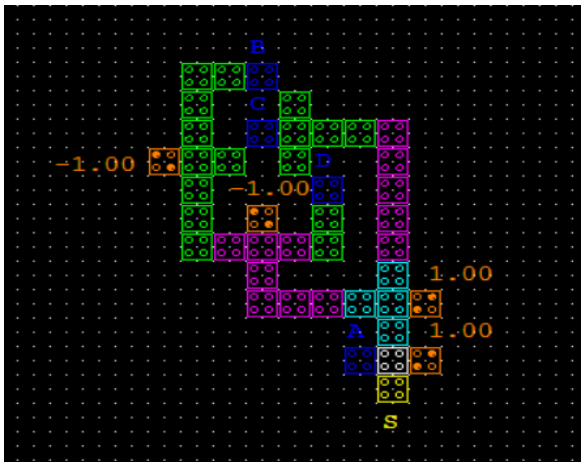

Fig. 16 QCA layout for the output S

For the output T: Figure 17 shows the designing of the output T in QCA technology. It is designed by using AND, OR and NOT gates. Clock 0 and 1 are used in the designing. B, C and D are the inputs whereas T is the desired output.

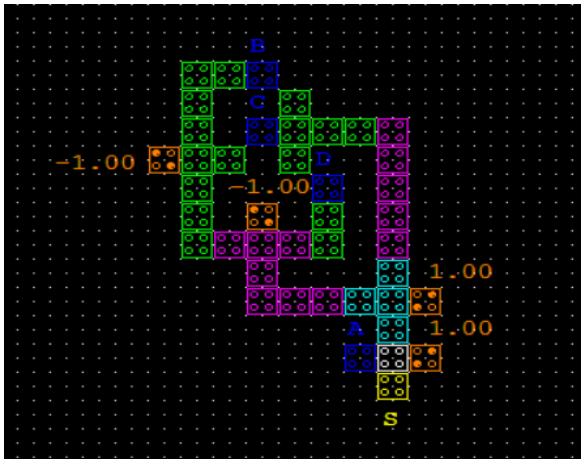

Fig. 17 QCA layout for the output T

For the output U: Figure 18 shows the designing of output U in QCA technology. It is designed by using OR and NNI gate. Clock 0 is used in the designing. A, B, C and D are the inputs whereas U is the desired output.

Fig. 18 QCA layout for the output U

For the output V: Figure 19 shows the designing of output V in QCA technology. It is designed by using OR and XOR gates. Clock 0, 1 and 2 are used in the designing. A, B, C and D are the inputs whereas V is the desired output.

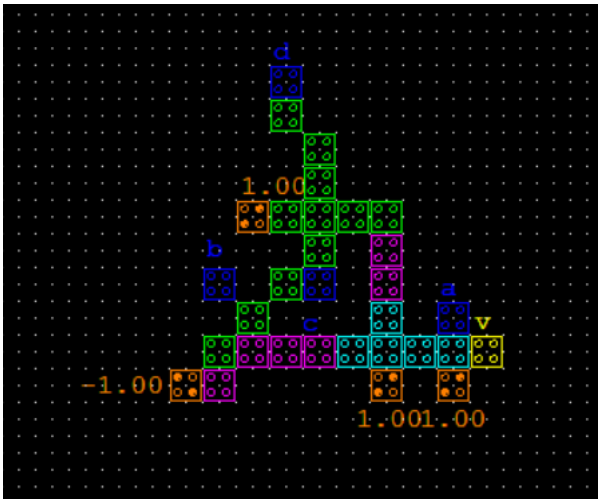

Fig. 19 QCA layout for the output V

IV. EXPERIMENTAL RESULTS

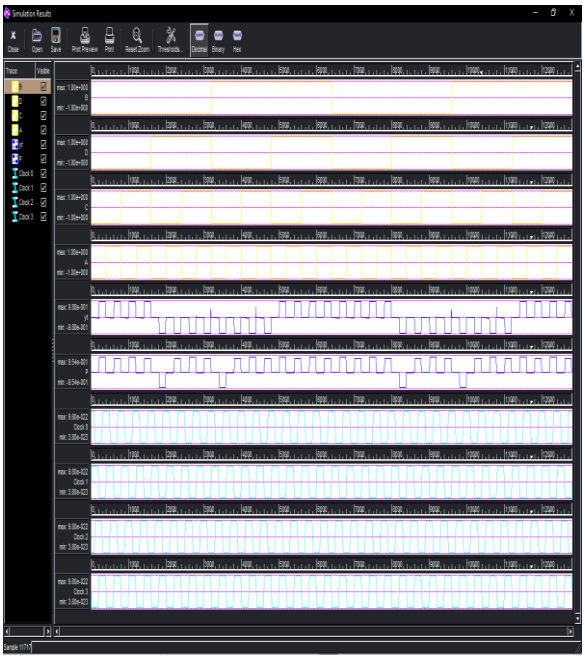

Fig. 20 Simulation of output P

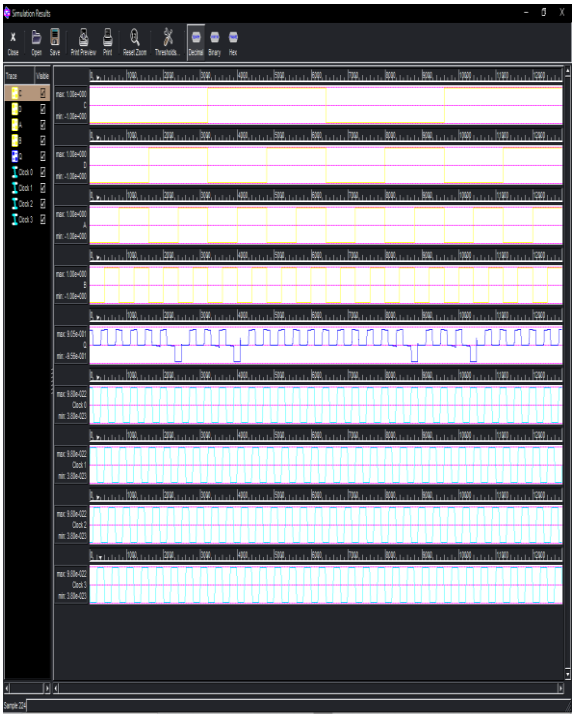

Fig. 21 Simulation of output Q

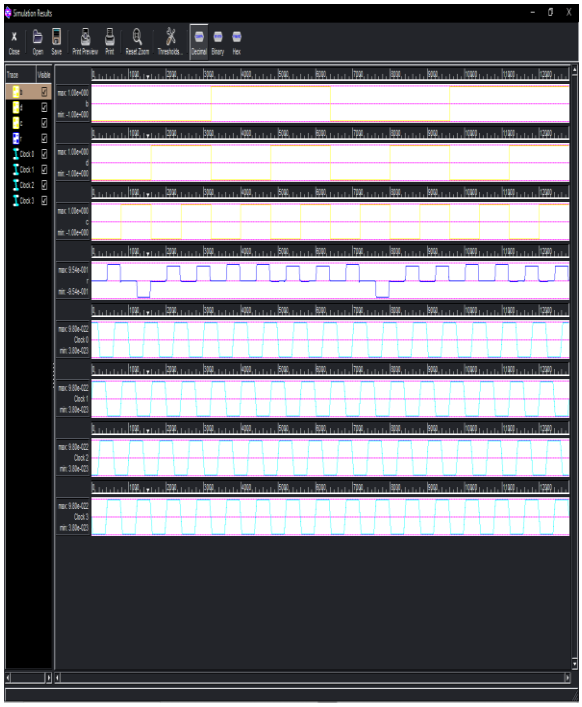

Fig. 22 Simulation of output R

Fig. 23 Simulation of output S

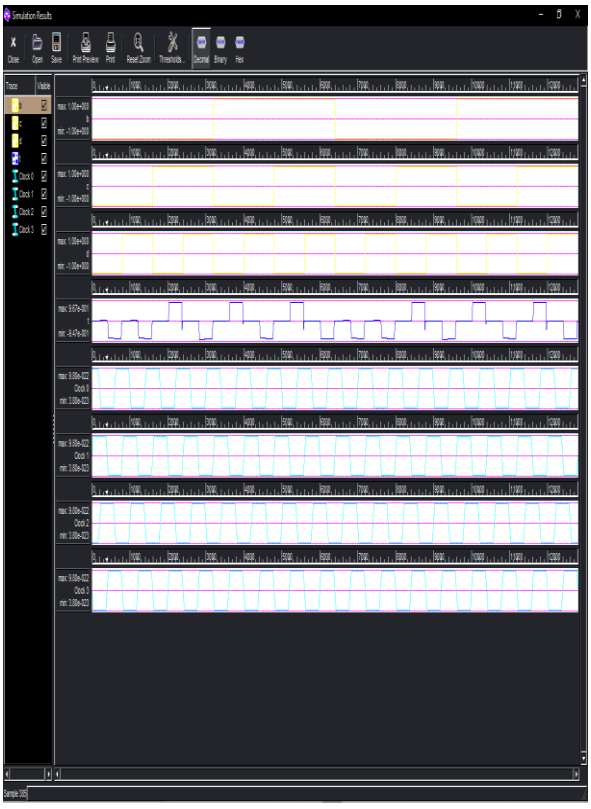

Fig. 24 Simulation of output T

Fig. 25 Simulation of output U

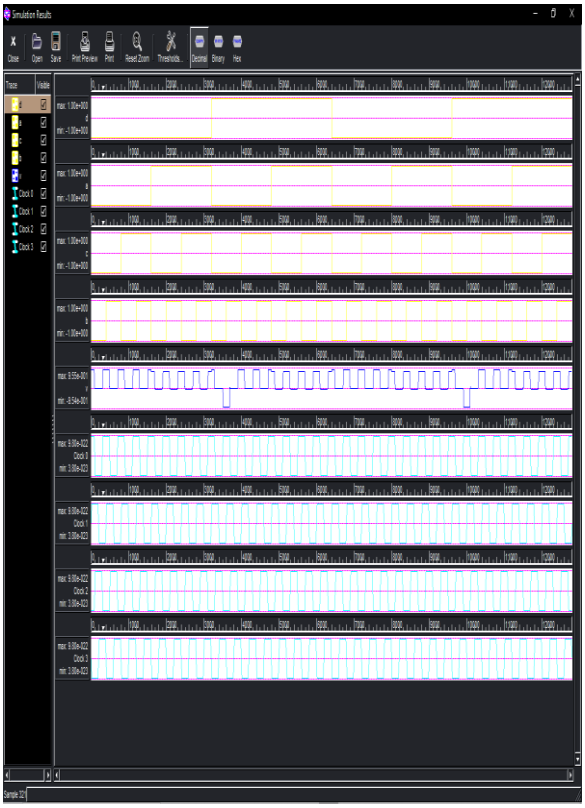

Fig. 26 Simulation of output V

V. CONCLUSION

In this paper an area efficient BCD to 7-segment decoder is designed which contains less number of QCA cells compared to existing design without altering the output. Also we achieve less delay which can be observed from the output waveform.

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