

# Decoupling of Power in A Solar PV System Employing A Partial Power Processing Converter

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## ABSTRACT

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To interconnect solar photovoltaic (PV) with the single phase grid, DC/AC inverters are used as interface. For tracking maximum power from each solar PV string, DC/DC converters are connected between solar PV strings and inverters. This ensures each string operates at its maximum power output irrespective of variation in solar radiation among different strings. Conventionally, DC-DC converter used for this application would process the complete power of the string. This full power processing (FPP), architecture leads to high conversion losses. This paper suggests a flyback based partial power processing converter, which offers high conversion efficiency, as compared to conventional dc-dc converters. In addition, the proposed scheme also eliminates low frequency (twice the power frequency) oscillations in string voltage in case of single phase inverters, thereby increasing the power extraction efficiency. Key advantages of the proposed scheme are power decoupling, low conversions losses, high extraction efficiency and distributed maximum power point tracking (DMPPT). Detailed simulation studies are performed to validate the performance of the proposed scheme. Comparison of the proposed scheme with the conventional full power processing scheme is also included.

**Index Terms** - DC-DC converter, distributed maximum power tracking (DMPPT), Partial power processing (PPP), maximum power point (MPP), partial shading, PV characteristics.

## I. INTRODUCTION

SOLAR PV enables distributed generation of clean and re-newable electricity. Various solar PV panels are connected

in series to increase the voltage level of the string. Multiple such strings are connected to a single solar PV inverter. The power-voltage characteristics for one string assuming solar radiation on all PV panels is equal, is shown in

Fig.1. Since, characteristics of all string are same, the tracking of maximum power point can be done by controlling the voltage of all the strings to a common value. In this case, all strings can be connected in parallel and fed to a common inverter [1]. However, in actual condition, few panels of a solar PV strings could be partially shaded [1]. The power-voltage characteristics of a string with 1 panel partially shaded (70% shaded) and other 9 panels receiving full radiations, is shown in Fig. 1. The voltage at which maximum power is available from this string is different from the corresponding voltage of a normal string. In this case, if a partially shaded string is connected in parallel to a normal string, only one of the string could be operated at its maximum power point (MPP).

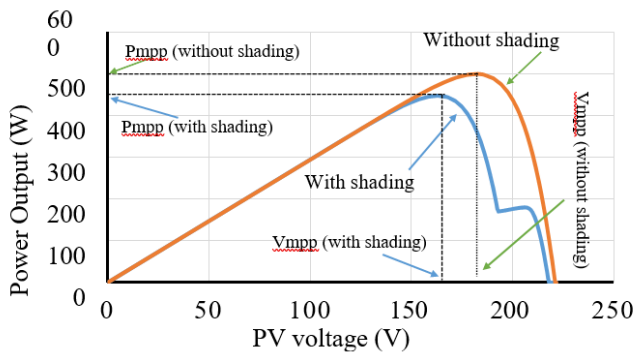


Fig. 1. Effect of partial shading on solar PV string characteristics. One module 70% shaded and rest nine receiving 100% radiation.

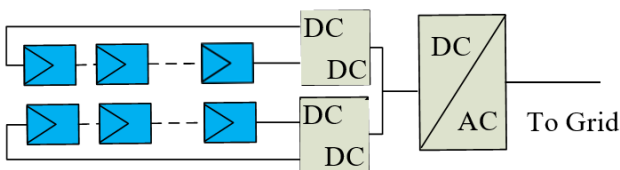


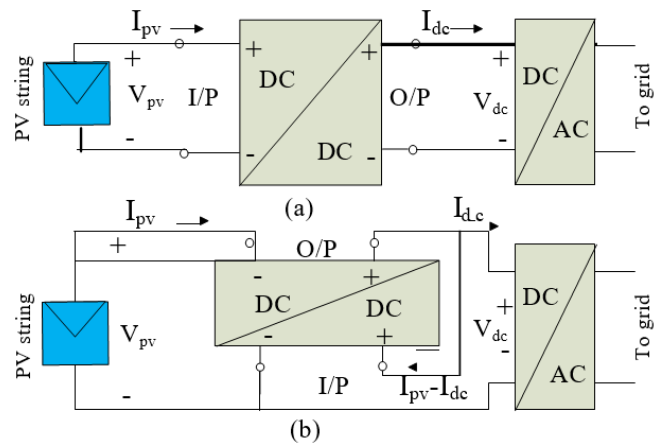
Fig. 2. String level distributed maximum power point tracking (DMMPT) architecture.

Therefore, this would lead to suboptimal utilization of solar PV panels.

To address the above issue of power mismatch due to partial shading, DC-DC converter is integrated at

either sub-array or string or module level. This approach is called distributed maximum power point tracking (DMPPT). To improve the overall system efficiency, various DMPPT PV system architectures have been reported in the literature [1]. It is analyzed in [1] that energy yield is highest for DMPPT at string level. String level maximum power point tracking (MPPT) using dc-dc converters for each string is shown in Fig. 2.

DC-DC converters used in the aforementioned application are categorized as: (i) full power processing (FPP) and (ii) partial power processing (PPP) architecture [2]. Fig. 3(a). shows the structure of FPP. In this case, complete output power of the solar PV string is processed by the converter. The use of Buck, boost, or buck-boost converter topology for FPP is investigated in detail in [3]. It is concluded that for a given cost, buck converter will be most efficient. To improve the efficiency and operation over wide range of PV voltage, a bridge based buck/boost topology is suggested in [4]. It can



operate in buck, boost and pass through mode. Even with no mismatch in the string, FPP converter need to process the whole PV power. This results in increased power loss.

In case of PPP architecture shown in Fig. 3(b), the major portion of solar PV power is directly fed to the inverter, thereby a considerably small amount of power need to be processed by the converter. The power processed by the converter is equal to the product of the solar PV string current and a small

voltage injected in series to the solar PV string. This results in lower power rating of the converter. Further, it may lead to lower conversion losses as compared to FPP. Also, in case of no mismatch between strings, PPP does not process any power, thereby increasing the overall efficiency. A buck-boost converter based PPP is suggested in [7]. The converter topology suggested is basically a FPP boost converter rather than PPP as analyzed in [8]. A flyback converter connected between PV module and dc bus based PPP is suggested in [9], [10]. Flyback converter injects a compensating current in parallel with the module to equalize the total module current to the string current. A high frequency transformer based phase shifted full bridge converter is suggested in [11]. The converter used is configured as PPP converter by feed forwarding the input power. Similarly, buck-boost based PPP topology and switched capacitor circuit are suggested in [12] and [13]- [14], respectively. A flyback converter based PPP suggested in [15], [16] injects voltage in series with the PV panel to adjust the mismatch. These module integrated PPP converter is generally connected to dc link of the single phase inverter. Due to single phase, the instantaneous power fed to grid oscillate at twice the grid frequency which results in twice the power frequency ripple in dc link voltage. The PPP suggested above are not designed to handle the voltage ripple causing decrease in power extraction efficiency of the PV system. The objective of the paper is to utilize flyback PPP to address the problem of partial shading at string level as well as to mitigate the extraction efficiency issue as a result of the voltage ripple at PV terminal.

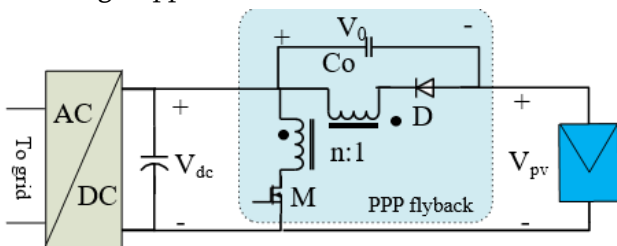


Fig. 4. PPP flyback topology

This paper is organized as follows. Section II presents the proposed PPP scheme and its control. In section III using analytical equations, efficiency of the proposed scheme is compared to that of a FPP boost converter scheme. Simulation result of the scheme is shown in section IV. Conclusions are reported in Section V.

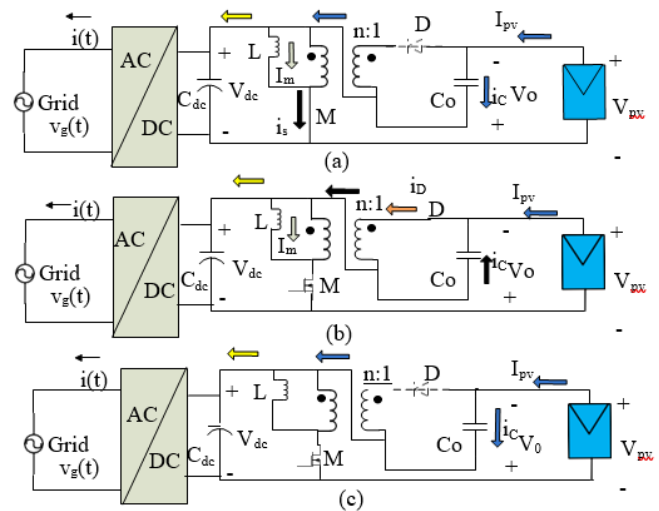


Fig 5. Stages of operation (a) Mode-1 (b) Mode-2 (c) Mode-3

## II. PROPOSED PPP SCHEME

### A. Circuit Topology

The circuit topology for PPP is shown in Fig. 4.  $V_{pv}$  and  $V_{dc}$  are PV MPP voltage and dc link voltage of inverter, respectively. To achieve PPP architecture, the input of flyback converter is connected to dc link of inverter and output of converter in series of the PV terminal. The operation of the converter is explained below:

**Mode 1** [ $0 < t \leq DT_s$ ], Fig. 5(a): When the power switch S is turned on, diode D is turned off by the reverse voltage of  $\{-n2 n1V_{dc} + V_o\}$ . This results in the build-up of the magnetizing inductor current. Also, the path of PV current is through the output capacitor of the converter ( $C_o$ ).

**Mode 2** [ $DT_s < t \leq D2T_s$ ], Fig. 5(b): In this mode, when switch S is turned off, diode D starts conducting to provide a path to the magnetizing current. The PV current finds two paths; one through the diode D and other through the output capacitor  $C_o$ . The capacitor  $C_o$  will charge in this interval.

**Mode 3** [ $D_2T_s < t \leq T_s$ ], Fig. 5(c): When the diode current reaches zero, the switch and diode stop conducting and PV current flow through the output capacitor  $C_o$ .

The current and voltage waveform for the proposed converter is shown in Fig. 6. Applying volt-second balance for magnetizing inductor gives the steady state relation:

$$V_o = \frac{V_{dc}D}{nD_2} \tag{1}$$

where,  $V_o$  and  $V_{dc}$  are output voltage of converter and dc link voltage of inverter, respectively,  $D$  and  $D_2$  are the duty ratio of switch and diode, respectively and  $n$  is the turn ratio of transformer. In steady state, average current through the capacitor  $C_o$  over a switching cycle is zero. This leads to,

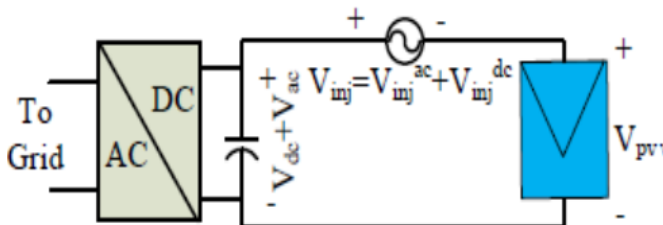
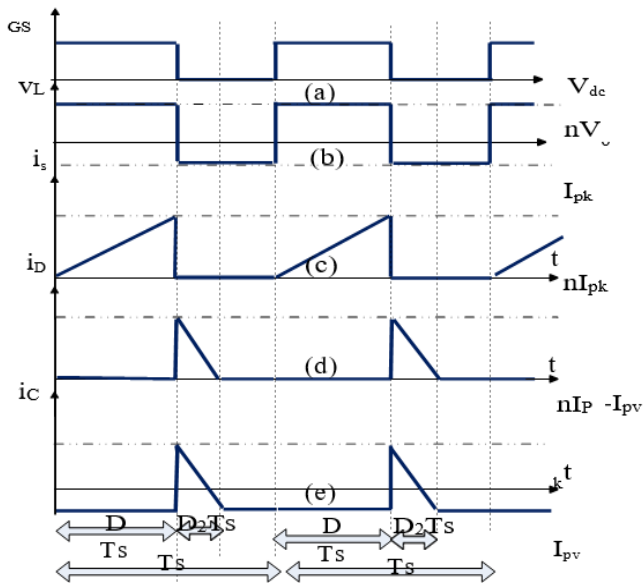


Fig 7. Schematic of the proposed concept

$$I_{pv} = (nD_2I_{pk})/2 \tag{2}$$

Using the magnetizing inductor equation,

$$I_{pk} = (V_{dc}DT_s)/L \tag{3}$$

Substituting  $I_{pk}$  from (3) to (2) and using (1),

$$D = \frac{\sqrt{2V_oI_{pv}Lf_s}}{V_{dc}} \tag{4}$$

$$D = \frac{2I_{pv}L}{nV_{dc}DT_s} \tag{5}$$

For discontinuous mode of operation ( $D + D_2 < 1$ ), value of magnetizing inductance is given by,

$$L < \frac{(nV_{dc})^2V_o}{2(V_{dc}+nV_o)^2I_{pv}f_s} \tag{6}$$

Value of the output capacitance considering  $x\%$  ripple in its voltage w.r.t PV voltage is given by,

$$C_o = \frac{nI_{pk}D_2}{x\%V_{pv}} \left\{ \frac{1}{2} - \frac{I_{pv}}{I_{pk}} \right\} \tag{7}$$

**B. Control of converter**

The concept is illustrated in Fig.7 where  $V_{inj}$  is the injected voltage by the fly back PPP converter.  $V_{inj}$  has two component:

- 1)  $V_{inj}^{dc}$  is the dc component of the injected voltage, which is calculated such that the total voltage seen by solar PV ( $V_{dc} - V_{inj}^{dc}$ ) is close to its maximum power point ( $V_{mpp}$ ).

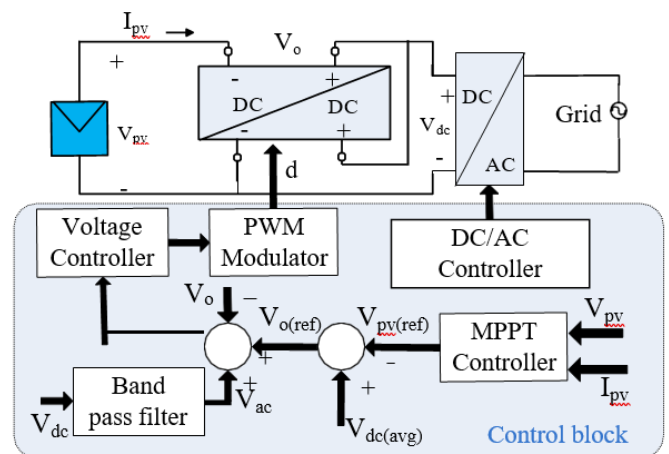


Fig. 8. Control block diagram for DMPPT and low frequency ripple cancellation

$V_{inj}^{ac}$  is injected 2nd harmonic ripple voltage at converter terminal output such that it cancels the 2nd harmonic voltage in the dc-link of the inverter, thereby ensuring no oscillations in dc voltage appearing across

solar PV.

The control block diagram for the PPP-based fly back converter is shown in Fig. 8.  $V_{pv}$  And  $I_{pv}$  are inputs to the MPPT controller, which provides reference value for solar PV string voltage,  $V_{pv(ref)}$ . Any conventional MPPT algorithm for partial shading can be used. The obtained  $V_{pv(ref)}$  is subtracted from the dc link voltage  $V_{dc(avg)}$  to obtain dc reference for  $V_o$ . Second harmonic component of the dc link voltage is extracted using band pass filter and added to  $V_{o(ref)}$  for comparison with  $V_o$  to generate error for voltage controller. The voltage controller parameter are selected that the bandwidth of the system (controller + plant) is more than 2nd harmonic, thereby ensuring unity gain at 2nd harmonic frequency in the closed loop transfer function. This results in the generation of harmonic component (opposite magnitude) at the fly back output. This ensures no oscillations in solar PV voltage as both the 2nd harmonic components (one of dc link and other of fly back) cancel each other. Since the converter output has ac component ( $V_{inj}^{dc}$ ) along with the dc voltage ( $V_{inj}^{ac}$ ), and fly back output cannot be negative, following relation should always hold for the output voltage:

$$V_{inj}^{dc}(t) + V_{inj}^{ac}(t) \geq 0 \tag{8}$$

The power processed by this fly back converter would be less in the case of small injection of voltage. This would ensure high efficiency of operation. To achieve this, the dc link voltage of the inverter is determined such that the following conditions are met:

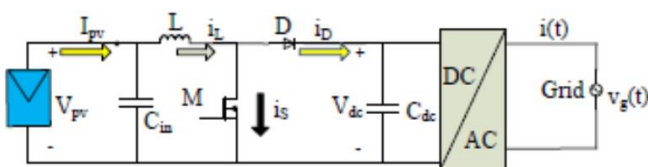


Fig.9 Boost Converter

TABLE I. SPECIFICATION OF SYSTEM

PARAMETER	VARIABLE	VALUE
Maximum power of string	$P_{MPP}$	1050 W
String Voltage at $P_{max}$	$V_{MPP}$	382.2 V
String Current at $P_{max}$	$I_{MPP}$	2.75 A
String Short Circuit Voltage	$I_{SC}$	2.95 A
String open circuit voltage	$V_{OC}$	464.4 A
Temperature coefficient of $V_{oc}$	A	0.081%
Temperature coefficient of $I_{sc}$	B	-0.37%
DC link voltage	$V_{dc}$	$\geq 374 V$
Switching frequency	$f_s$	100KHZ

- 1) The string with highest MPP voltage will decide the dc link voltage (equation (8) is to be satisfied).
- 2) The other dc/dc converter output is adjusted accordingly to operate each string at its MPP.
- 3) The minimum dc link voltage is limited by the grid voltage.

### III. COMPARISON WITH BOOST TOPOLOGY

In this section, the partial power processing flies back converter is compared with the boost converter topology.

#### A. STEPS FOR EFFICIENCY EVALUATION

Steps for evaluating efficiency of the converter at different operating condition is listed as

- 1) PV string is simulated to obtain MPP voltage and current for different temperature and radiation level.
- 2) DC link voltage and required injected voltage for fly back configuration are decided.
- 3) Based on the above selection, semiconductor devices and other component are selected.
- 4) Losses are estimated for different operating conditions.
- 5) Efficiency curve are plotted for  $I_{mpp}$  and  $V_{mpp}$  variation.



6) CORE LOSS: The magnetic core loss for a ferrite core is given by

TABLE II. SELECTED COMPONENT FOR COMPARISON

COMPONENT	PPP FLY BACK CONVERTER	FPP BOOST CONVERTER
MOSFET	Max voltage stress = 1088 V Max current rating = 0.6 A Selected STFW4N150 (1500 V and 4 A rating)	Max voltage stress = 400 V Mac current rating =0.89A Selected STB6NK60Z (600 V and 4 A rating)
Diode	Max voltage stress = 197 V Max current rating = 2.7 A Selected STTH10R04 (400 V and 10 A rating)	Max voltage stress = 400 V Max current rating = 2.72 A Selected STTHA008DTI (800 V and 10 A rating)
Magnetics required	Transformer turns ratio 5:1 Mag. Inductance 0.6737 mH	Inductance 0.9194 mH
Core	EE 20b 95 Primary wdg (2 strands) 6 secondary wdg (10 stands)	EE-25core 241 turns (3 strands)
Output Capacitor	23.14μF	-

Table I summarize the specification of PV panel. Based on design requirement semiconductor component and passive element used in both PPP fly back and FPP boost converter are Tabulated in table II

B.Loss Calculation

This section discusses the equations used for determining the various losses in the system:

1) MOSFET CONDUCTION LOSS:

In the on-state MOSFET exhibit a finite resistance. When the device conduct this results in conduction power loss. Based on the waveform for current through switches, RMS current is calculated. The RMS value of switch current in boost converter and fly back converter is given by (9) and (10), respectively.

$$I_{rms}^B = I_{pv} \sqrt{D \left\{ 1 + \frac{1}{3} \left( \frac{\Delta i}{I_{pv}} \right)^2 \right\}} \tag{9}$$

$$I_{rms}^F = \frac{2I_{pv}}{nD_2} \sqrt{D/3} \tag{10}$$

Conduction loss is obtained by the square of the RMS current multiplied by the Rds.

2) MOSFET SWITCHING LOSS:

For estimation of switching loss, switching trajectory is considered linear. Switching loss (turn-on and turn-off losses) of MOSFET are given by,

$$P_M = V_{ds} I_{Don} \frac{tri+tfu}{2} f_s + V_{ds} I_{Doff} \frac{tru+tfi}{2} f_s \tag{11}$$

where tri = rise time to be obtained from the datasheet  
tfu = voltage fall time

$$= (V_{ds} - R_{dspn} I_{Dpn}) \cdot R_G \frac{U_{GD(avg)}}{U_{dr} - U_{pleatue}}$$

tru = voltage rise time

$$= (V_{ds} - R_{dson} I_{Doff}) \cdot R_G \frac{C_{GD(avg)}}{-U_{(pleatue)}}$$

V<sub>ds</sub> and I<sub>Don</sub> I<sub>Doff</sub> are input voltage and current just before turn on and turn off, respectively.

3) DIODE CONDUCTION LOSS:

Diode conduction loss is calculated from the expression

$$P_D = V_f I_{f(avg)} + R_f I_f^2(rms) \tag{12}$$

For boost converter, RMS value of diode current is given by,

$$I_{f(rms)} = I_{pv} \sqrt{(1 - D) \left\{ 1 + \frac{1}{3} \left( \frac{\Delta i}{I_{pv}} \right)^2 \right\}} \tag{13}$$

and for flyback converter, it is given by,

$$I_{f(rms)} = \frac{2I_{pv}}{D_2} \sqrt{\frac{D_2}{3}} \tag{14}$$

4) WINDING COPPER LOSS:

Due to the finite resistance of primary and secondary winding, power is dissipated in the form of heat. The expression of primary and secondary winding losses of fly back are given by Pp = I<sub>2</sub> F<sub>rms</sub> R<sub>p</sub> and Ps = I<sub>2</sub> F<sub>rms</sub>Rs. For the inductor of boost converter, loss is given by Pl = I<sub>2</sub>B<sub>rms</sub> Rind. The temperature effect on the copper loss is neglected

5) CORE LOSS: The magnetic core loss for a ferrite core is given by,

$$P_{core} = \frac{k f^m B^n W}{K_g} \tag{15}$$

The constant k, m and n depend on the material used. For selected material [19]: m=1.63, n=2.62, k=4.855.10<sup>-5</sup>, B<sub>ac</sub>=Peak flux density (T). W/Kg= core weight

C. EFFICIENCY COMPARISON

Two strings connected in parallel to a common dc link with dc-dc converter are selected such that one

string is receiving full radiation and other is partially shaded. The unshaded string irradiance level is fixed at 1000 W/m<sup>2</sup>. Since the dc link voltage would be determined by this string it is fixed to 400 V (equal to the sum of MPP voltage of non-shaded string (382.2 V) and the peak of the second harmonic ripple in dc link). The partially shaded string irradiance level is From 200 W/m<sup>2</sup> to 1000 W/m<sup>2</sup> in step of 100 W/m<sup>2</sup>. This variation in radiation would result in different MPP voltage and MPP current. The shaded panel dc-dc converter operates to make the panel work at its MPP. For each radiation level, the efficiency of the converter is calculated. This process is repeated for different panel temperature. Efficiency plot with FPP boost and PPP fly back converters of the shaded string is obtained. Figs.10 (a) and 10(b) shows the plot of efficiency verses MPP current and MPP voltage, respectively for different panel temperature. From the efficiency plot, it is observed that if MPP voltage changes by a small value (reduces by a small value from MPP voltage at STC (382.2 V)) due to radiation, PPP fly back is more efficient.  $I_{mpp}$  would reduce with shading. It is observed that, up to 50% shading of the string at a temperature of 40°C, the fly back PPP would be more efficiency than boost FPP. In extreme case when one of the string is non shaded and other is shaded by more than 50%, boost would offer higher efficiency. However, occurrence of partial shading among the strings is more likely then complete shading of one of the string. Therefore, the proposed topology would be more efficient in handling the mismatch that happen due to partial shading of some module for parallel strings configuration.

**IV. SIMULATION RESULTS**

In order to valid the effectiveness of the topology in mitigat- ing the mismatch in paralleled connected strings, two strings with proposed PPP are simulated in MATLAB/Simulink envi- ronment. The simulated

system is shown in Fig. 2 and system specifications are listed in Table. I. Three cases are considered:

A. Case 1: When none of the strings are partially shaded.

When both of the strings receive equal radiation without any partial shading (PV MPP voltage=382.2 V), the PPP converter function is to only inject the 2nd harmonic ripple voltage magnitude in opposite to the dc link ripple. For this case, dc link voltage is maintained constant at 400 V. The PV voltage and the injected ripple voltage for the string-1 and string-2 are shown in Fig. 11. It is clear that the converter is able to neutralize the 2nd harmonic ripple effect on PV panel.

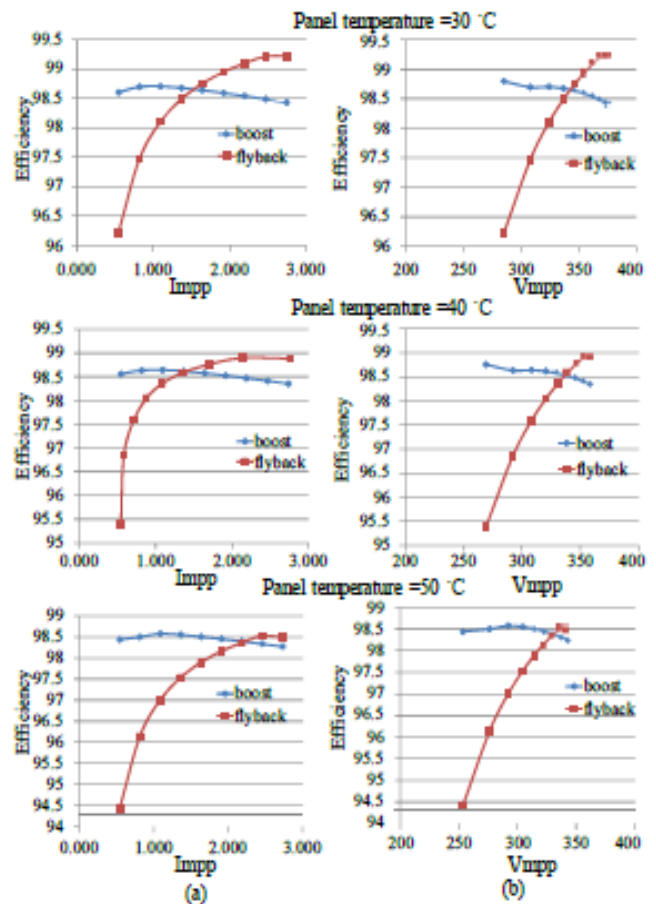


Fig. 10 Efficiency plot at different panel temperature (a) for  $I_{mpp}$  variation (b) for  $V_{mpp}$  variation

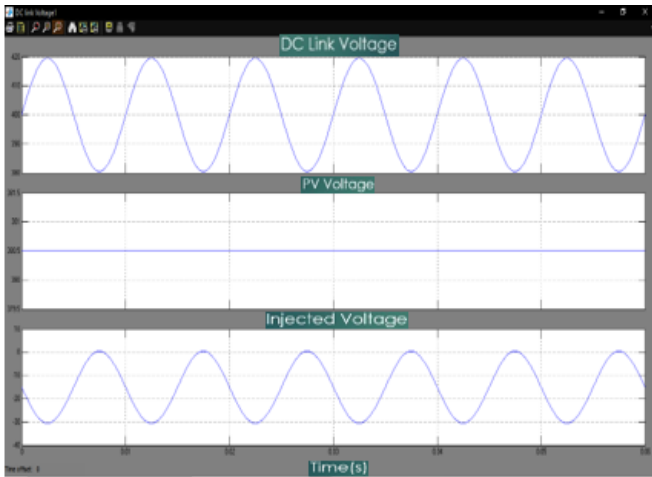


Fig. 11. Case 1: DC link voltage, PV terminal voltage and injected voltage for string 1 and 2

B. Case 2: When one string is partially shaded.

String-1 is partially shaded and no module of string-2 is shaded. Since the 2nd harmonic ripple voltage is 26.52 V peak to peak, the dc link voltage is set to 374 V so as to make the string-2 operate at its MPP voltage (357.67 V). This is achieved by PPP converter of string-2 by injecting the 2<sup>nd</sup> harmonic ripple at its output. Due to shading, the string-1 MPP voltage is lowered to 338.85 V. The converter of the string-1 injects the difference voltage and the 2nd harmonic ripple at its output to match to the dc link voltage. This is illustrated in the simulation result shown in Fig.12 (a) and (b).

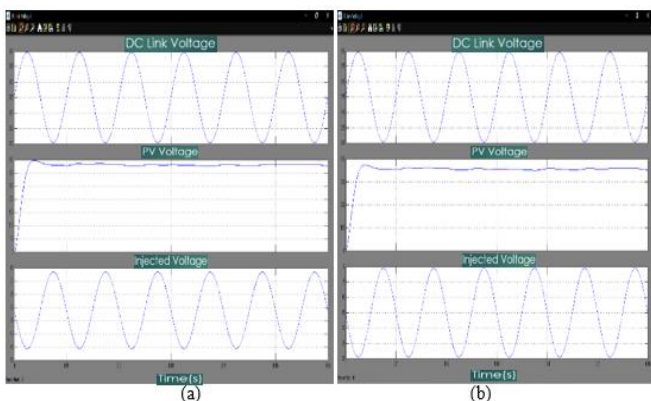


Fig. 12. Case 2: (a) DC link voltage, PV terminal voltage and injected voltage for string 1. (b) DC link voltage, PV terminal voltage and injected voltage for string 2.

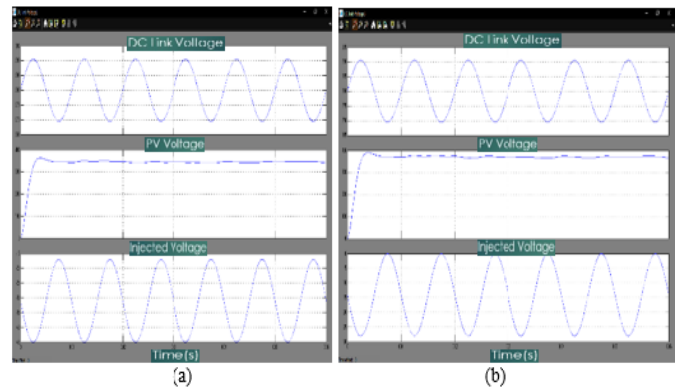


Fig. 13. Case 3 : (a) DC link voltage, PV terminal voltage and injected voltage for string 1. (b) DC link voltage, PV terminal voltage and injected voltage for string 2.

C. Case 3: When both strings are partially shaded

For this case both the strings have some modules partially shaded making the MPP voltage of string 1 as 346.72 V and string 2 as 368.49 V. DC link voltage is lowered to 381 V. This result in 2nd harmonic ripple voltage of 23.07 V peak to peak at dc link. The respective PPP converter develops the difference voltage to fully utilize the strings at its MPP point. This is illustrated in the simulation result shown in Fig 13 (a) and (b).

## V. CONCLUSION

This paper suggests a flyback partial power processing (PPP) topology. The converter injects a series voltage which has two component. DC component of output voltage handles the string mismatch with dc link and ac component cancel the effect of 2nd harmonic voltage oscillation of the dc link at PV terminal. Converter parameter design and control aspects are discussed. As a result of partial shading in panels MPP current changes considerably. Efficiency calculation shows that PPP flyback is more efficient than full power processing scheme based on boost converter for partial shading of less than 50% at panel temperature of 40°C. Simulation result for different case of shading is



included to verify the operation of the proposed scheme.

## VI. REFERENCES

- [1]. A. Elasser et al. "A Comparative Study of Central and Distributed MPPT Architectures for Megawatt Utility and Large Scale Commercial Photovoltaic Plants," Proceedings of Ind. Electron. Conference, IECON 2010, pp. 2753-2758.
- [2]. M. Kasper, D. Bortis, J.W.Kolar, "Classification and Comparative Evaluation of PV Panel-Integrated DC/DC Converter Concepts," IEEE Trans. Power Electron., vol. 29, no. 5, pp. 2511-2526, May. 2014.
- [3]. G. R. Walker and P. C. Sernia, "Cascaded dcdc converter connection of photovoltaic modules," IEEE Trans. Power Electron., vol. 19, no. 4, pp. 1130-1139, Jul. 2004.
- [4]. G. R. Walker and J. Pierce, "PhotoVoltaic DC-DC Module integrated Converter for Novel Cascade and Bypass Grid Connection topologies- Design and optimisation," in Proc. of Power Electron. Specialist. Conf. PESC 2006, pp. 1-7, 18-22 June 2006.
- [5]. G. Yao, L. Hu, Y. Liu, L. Chen, and X. He, "Interleaved Three-Level Boost Converter with Zero Diode Reverse Recovery Loss," in Proc. of Applied Power Electronics Conference (APEC) 2004, pp. 1090-1095
- [6]. R. Steigerwald, "A Comparison of Half-Bridge Resonant Converter Topologies," IEEE Trans. Power Electron., Vol. 3, No. 2, pp. 174-182, April 1988.
- [7]. M.S Agamy et al., "An Efficient Partial Power Processing DC/DC Converter for Distributed PV Architectures," IEEE Trans. Power Electron., vol. 29, no. 2, pp. 674-686, Feb. 2014. T. Suntio and A. Kuperman, "Comments on An Efficient Partial Power Processing DC/DC Converter for Distributed PV Architectures," IEEE Trans. Power Electron., vol. 30, no. 4, pp. 2372-2372, April 2015.
- [8]. P. S. Shenoy, K. A. Kim, B. B. Johnson, and P.T.Krein, "Differential power processing for increased energy production and reliability of photovoltaic systems," IEEE Trans. Power Electron., vol. 28, no. 6, pp. 2968-2979, Jun. 2013.
- [9]. C. Olalla, D. Clement, M. Rodriguez, and D. Maksimovic, "Architectures and control of submodule integrated DC-DC converters for photovoltaic applications," IEEE Trans. Power Electron., vol. 28, no. 6, pp. 2980-2997, Jun. 2013.
- [10]. J. Lee, B. Min, T. Kim, D. Yoo, and J. Yoo, "High Efficient Interleaved Input-Series-Output-Parallel-Connected DC/DC Converter for Photovoltaic Power Conditioning System," in Proc. of Energy Conver. Conf. and Expo, ECCE 2009, pp. 327-329.
- [11]. C. Schaefer, K. Kesarwani, and J. T. Stauth, "A coupled-inductor multi-level ladder converter for sub-module PV power management," in Proc. IEEE Appl. Power Electron. Conf., 2013, pp. 732-737.
- [12]. S. Ben-Yaakov, A. Blumenfeld, A. Cervera, and M. Evzelman, "Design and evaluation of a modular resonant switched capacitors equalizer for PV panels," in Proc. IEEE Energy Convers. Congr. Expo., 2012, pp. 4129-4136.
- [13]. J. T. Stauth, M. Seeman, and K. Kesarwani, "Resonant switched-capacitor converters for sub-module distributed photovoltaic power management," IEEE Trans. Power Electron., vol. 28, no. 3, pp. 1189-1198, Mar. 2013.
- [14]. Junjian Zhao; K. Yeates, Yehui Han, "Analysis of high efficiency DC/DC converter processing partial input/output power," IEEE 14th Workshop on Control and Modeling for Power Electron., COMPEL, vol. 28, 23-26 June. 2013, pp. 1-8.

- [15]. Ho-sung kim, Jong-Hyun Kim, Byung-Duk Min, Dong-Wook Yoo, and Hee-Je Kim, "A highly efficient PV system using a series connection of DCDC converter output with a photovoltaic panel," Renewable Energy, vol. 34, Issue 11, pp. 24322436, Sept. 2009.
- [16]. A. Bidram, A. Davoudi, R.S. Balog, "Control and Circuit Techniques to Mitigate Partial Shading Effects in Photovoltaic Arrays," IEEE J. Photovoltaics, vol. 2, no. 4, pp.532-546, Oct. 2012
- [17]. D. Graovac, M. Purschel, A. Kiep, "MOSFET power losses calculation using the data-sheet parameters," Application Note, vol. 1.1, Jul. 2006.
- [18]. W.T. Mclyman, "Transformer and inductor design handbook," Third Edition, Kg Magnetics, Inc., USA 2004.

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