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Cost Efficient Designing of Quantum Cellular Automata Based Code Converters

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ABSTRACT

Intake manifolds have to be designed to improve engine performance by avoiding the phenomena like inter-cylinder robbery of charge, inertia of the flow in the individual branch pipes, resonance of the air masses in the pipes and the Helmholtz effect. The objective of work is to predict and analyze the flow through intake manifold of four cylinder spark ignition engine. One of the important factors is runner. The steady state analysis has been carried out for three for All runners open, The predicted results of total pressure loss and total outlet mass flow were discussed. Inlet pipe and plenum connection creates a back step geometry which causes more total pressure loss due to flow recirculation in conventional model. Tapering the geometry is causing more inlet mass flow due to reduction in total pressure loss in the plenum chamber.

Keywords: Fluent, Intake, Manifold, Runners

I. INTRODUCTION

QCA uses the paired order of quantum dots to implement the Boolean QCA (Quantum-dot Cellular Automata) is one of the most attractive alternatives for CMOS technology. QCA uses the paired order of quantum dots to implement the Boolean logic functions. QCA is physical implementation of a classic cellular automata from mechanic quantum effect.

The common digital technologies use the voltage or current ranges for showing the logic values, whilst in QCA technology, the situation of electrons in quantum dots shows the binary values.

The advantages of this technology include:

1. High operational speed (Tera Hertz range)
2. Low power consumption (approximately 100)
3. High device density

Minimum feature in CMOS has reduced after several decades, however, facing some limitation. This subject caused the rapid development of molecular plans in Nano- scale. QCA is a hopeful sample in nanotechnology, suggested by Lent et al. and created in 1997.

According to the considerable features of QCA such as high density, low power consumption, high speed

function potential and pipeline being advantage, QCA is changed as an interesting alternative technology for CMOS technology.

QCA is based upon encoding of binary information in the charge configuration within Quantum-dot cells. Computational power is provided by the Columbic interaction between QCA cells. No current flows between cells and no power or information is delivered to internal cells. The interconnection between QCA cells is provided by cell-to-cell interaction due to the rearrangement of electron positions .The two electrons are loaded in antipodal sides in Quantum-dots of a QCA cell.

A standard QCA cell is constituted of four quantum dots at four corners of a square cell. In this cell, four quantum dots have been paired together by the tunnel barriers. Two electrons existing in each cell may tunnel between the quantum dots inside the cell.

The high intercellular potential barriers ensure that no electron tunnels between QCA cells. Figure shows a standard QCA cell with four quantum dots located at its corners.

The efficacy of columbic interaction have run two electrons each to the cell diameters. The polarization of both stable states in cell diameters provides binary logic 0 and binary logic 1.

Figure exhibits the state of electrons placed in cell diameters and 0 and 1 binary information. If two cells are located next to each other, the columbic interaction between the electrons causes the cells to have equal polarization and the same value of its left side cell.

In Fig. some of QCA cells have been located beside each other and formed a wire in

QCA. In QCA technique, the wires are 45 and 90 degrees. Both wire types are used in the cross over and arrays intensively.

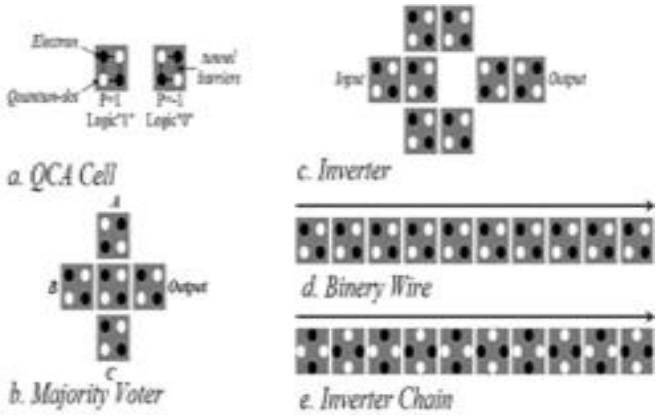

Fig. 1 a) QCA cell b) Majority Voter c) Inverter d) Binary Wire e) Inverted Chain

QCA clocking has been performed through timing in four distinct phases and required for both combinational and sequential circuits. Clocking not only controls the data current but provides the actual power in QCA circuits. The clock used in QCA consists of 4 phases: Switch, Hold, Release and Relax.

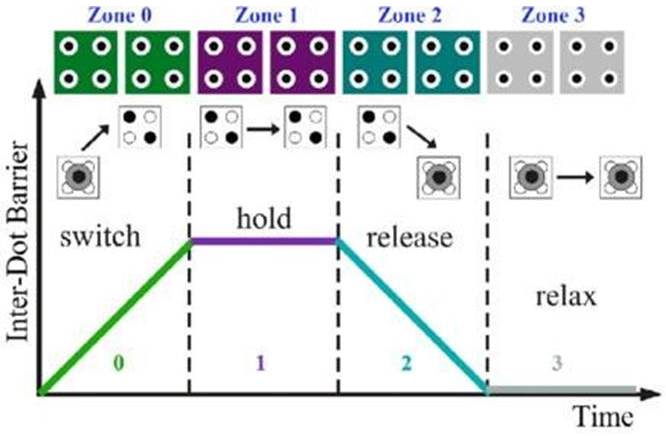

Fig. 2 QCA Clock Schemes

The signal energy lost by the medium is recovered by a new clocking. In QCA, clocking signals have been generated by an electrical field so that to control tunnel barriers in the quantum dots inside a QCA cell.

Quantum-dot cells are key components of QCA technologies to implement as Logic Gates, Wires, and Memories. The basic logic elements in QCA technology are the Majority gate and Inverter.

Wires can be used for signal propagation in QCA circuits.

Logic elements such as AND gate & OR gate can be obtained by manipulating the Majority gate.

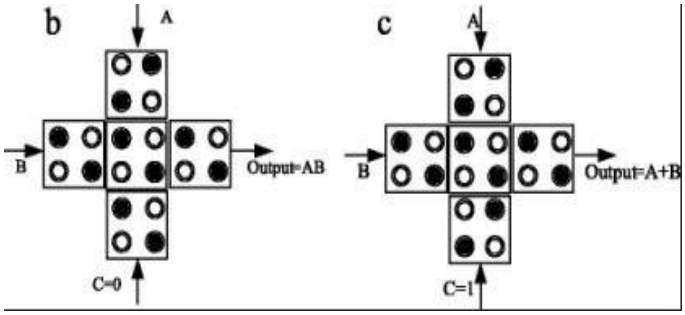

Fig. 3 AND & OR Gate Though the technology is different from convention CMOS designs, it is effective and realistic to implement the low power logic circuits. Thus, QCA is a new innovation at Nano-scale and an appealing substitute to ordinary CMOS. It is a possible technology for the next generation of digital circuits and systems and widely utilized as a part of advanced frameworks.

EARLIER WORK

The QCA computation proceeds by cell direction dependent on neighboring cell polarization. Estimates are designed for understanding the appropriate techniques and promoting the strategy proposed. QCA Designer is chosen at that level. QCA Designer reinforces the usefulness of the aim, which contains default values such as cell count.

Code converters are Circuits for interpreting a provided code into another, which is concealed in the logical array & run in a few regions toenhance the adaptability for information and hold outsiders informed. Binary code is how communication takes place and obtains user data using the number system. For example, the seven-bit binary sequence 1,100,100 is identical to the decimal number 100.

Gray code, being a numeral scheme, is defined by differing each value only by a single number from the previous number. Gray code is a numeral structure program where each value differs from the previous number. The gray code, which functions as an analog-to-digital converter has various useful uses; simplifies fault detection and peripheral tools

Binary to Gray converter:

A Binary to Gray Code Converter is a combinational logic circuit that converts a binary number to its equivalent gray code which is a non-weighted code. To convert binary to gray code, consider the significant most digit of the given binary number, as the significant most digit of the gray code number is almost similar as in the binary code. The biggest benefit is the very low amount of power consumption.

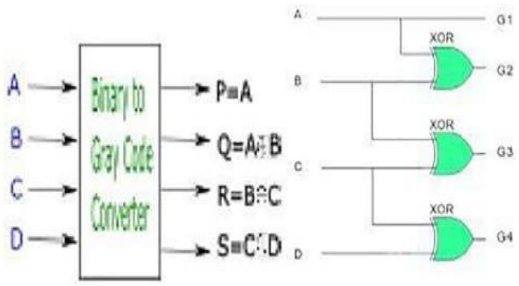

Fig: 4 Binary to gray code converter Table 1 describes the output combination for the sequence of inputs, in form of a truth table for a converter of 4- bit binary to gray code converter.

Table 1
Truth Table for Binary to Gray Code converter.

Truth Table							
Input Binary Code				Output Gray Code			
D	C	B	A	G4	G3	G2	G1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

On observing the truth Table 1, the outputs can be expressed as:

$G1 = A$

$G2 = A \text{ XOR } B$

$G3 = B \text{ XOR } C$

$G4 = C \text{ XOR } D$

Accordingly, the set of inputs and outputs are depicted which represents the block diagram of the converter from binary to gray code along with the circuit diagram. It is clear that the design of code converter (Binary to Gray code) circuit we applied XOR gate. So, an efficient XOR gate design will serve the purpose.

In this regard, we have chosen the design for the XOR gate. The XOR design was chosen for its property like low power consumption, performance in different order than the conventional design using cell interaction as shown in Fig. 5.

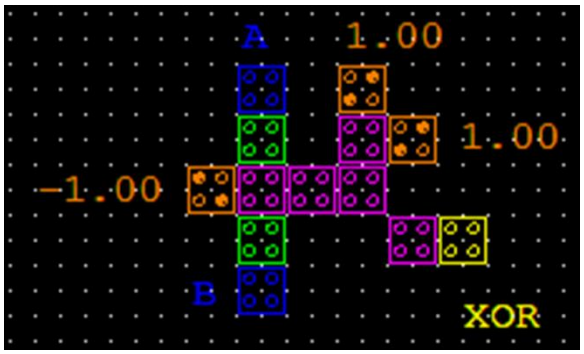

Fig.5: XOR design

The exact same XOR gate is implemented for the design of gray to binary code converter also. With these design principles, the QCA layout and the simulation wave form for the same are depicted Binary to Gray code converter. The design is entirely utilizing the property of the cell level methodology of QCA. It does not help to design an ultra-low power-based model, also reduces the necessary clock cycle in producing the result.

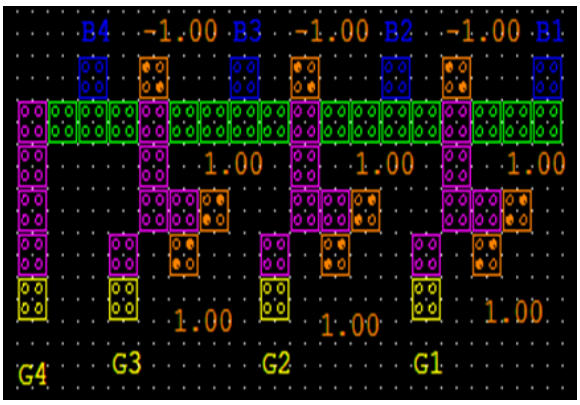

Fig.6: QCA design for binary to gray

This in terms reduces the QCA cost of the circuit and makes the design an efficient one. The design is completely using the property of cell-level methodology of QCA.

A Gray to Binary code Converter is a combinational logic circuit that transforms a Gray code to it equivalent binary code.

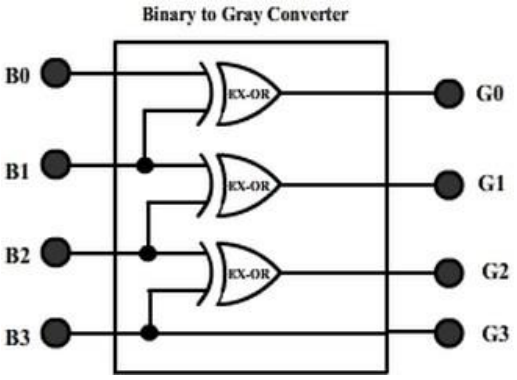

Fig.7

Table2 represents the truth table for a 4- bit Gray Code to Binary converter.

Table 2
Truth Table Gray to Binary Code converter

Truth Table							
Input Gray Code				Output Binary Code			
A	B	C	D	G1	G2	G3	G4
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Accordingly, the set of inputs and outputs are depicted, which presents the block diagram of gray to binary code converter and represented the circuit diagram of Gray to Binary code converter. On observing the truth Table 2, the outputs can be expressed as:

$B3 = G3$

$B2 = G \text{ XOR } G2$

$B1 - G \text{ XOR } GXOR \text{ } G1$

$B0 = G3 \text{ XOR } G2 \text{ XOR } G1 \text{ XOR } G0$

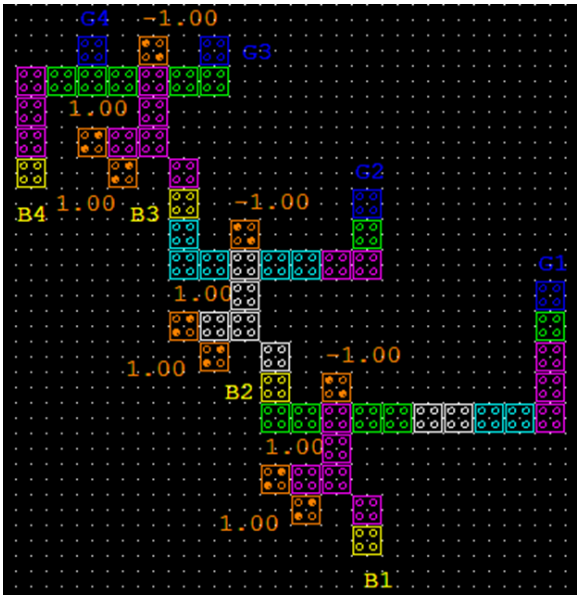

Fig. 8: Gray to binary code converter

PROPOSED WORK

The existing code convertors design uses XOR gates which consists of more number of QCA cells which is a major drawback in the design. In the proposed design an area efficient XOR gate is implemented which significantly reduces the total number of QCA cells in code convertors.

Binary to Gray converter: A Binary to Graycode converter is a combinational logic circuit that transforms a binary code to it equivalent gray code.
Block diagram of binary to gray code convertor is shown in fig.5
The truth table for binary to gray code convertor is shown in table 3.

Truth Table for Binary to Gray Code converter.

Truth Table

Input Binary Code				Output Gray Code			
D	C	B	A	G4	G3	G2	G1
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Table 3

The output of 4- bit binary to gray code converter can be expressed as:

G1 = A

G2 = A XOR B

G3 = B XOR C

G4 = C XOR D

The proposed area efficient XOR design was chosen for its better performance instead of conventional design using cell interaction as shown in Fig.9

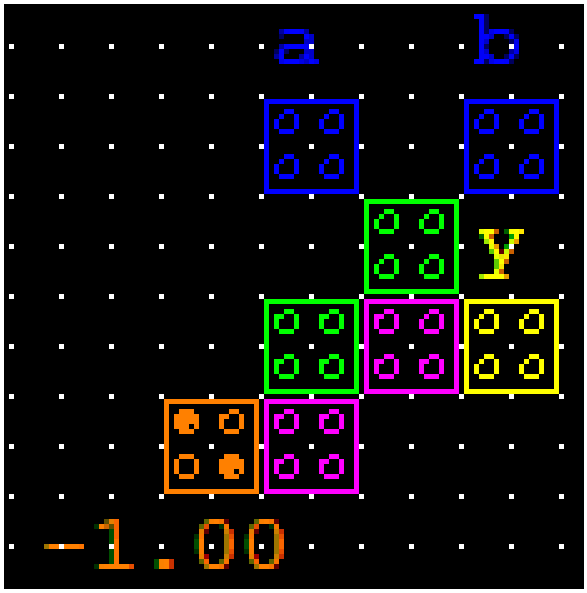

Fig.9 XOR

By using the proposed XOR gate binary to gray code convertor is designed which can be seen in fig.10

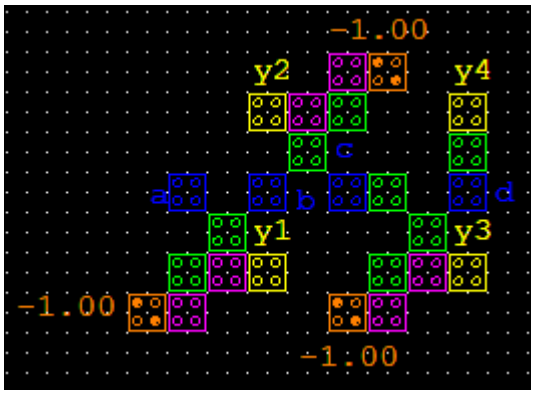

Fig.10 Binary to Gray code convertor As the number of cells are reduced which in terms reduces the QCA cost of the circuit and makes the design an efficient one. The design is completely using the property of cell-level methodology of QCA.

Gray to Binary converter: A Gray to Binary code Converter is a combinational logic circuit that transforms a Gray code to it equivalent binary code.

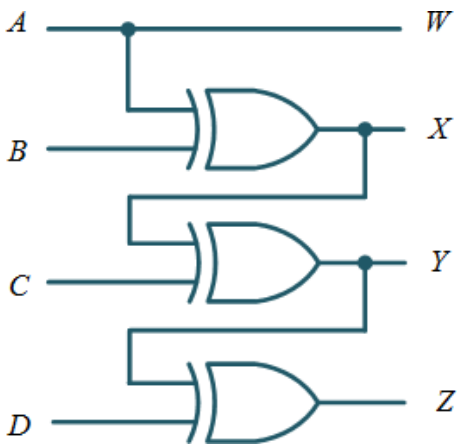

Fig.11 Block Diagram of Gray to Binary converter
The outputs can be expressed as:

$$B3 = G3$$

$$B2 = G \text{ XOR } G2$$

$$B1 - G \text{ XOR GXOR } G1$$

$$B0 = G3 \text{ XOR } G2 \text{ XOR } G1 \text{ XOR } G0$$

Table represents the truth table for a 4-bit Gray Code to Binary converter.

Truth Table Gray to Binary Code converter

Truth Table

Input Gray Code				Output Binary Code			
A	B	C	D	G1	G2	G3	G4
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Table 4

By using the same proposed XOR gate we can also implement gray to binary code convertor as shown in fig.12

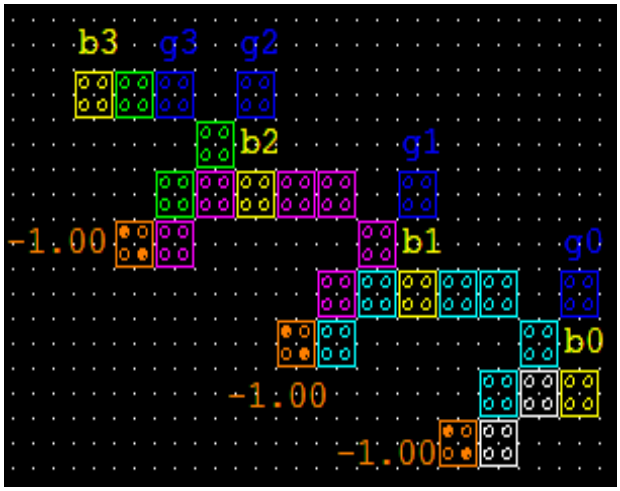

Fig.12 Gray to Binary converter in QCA

EXPERIMENTAL RESULTS

The simulation output for the proposed XOR gate is shown below.

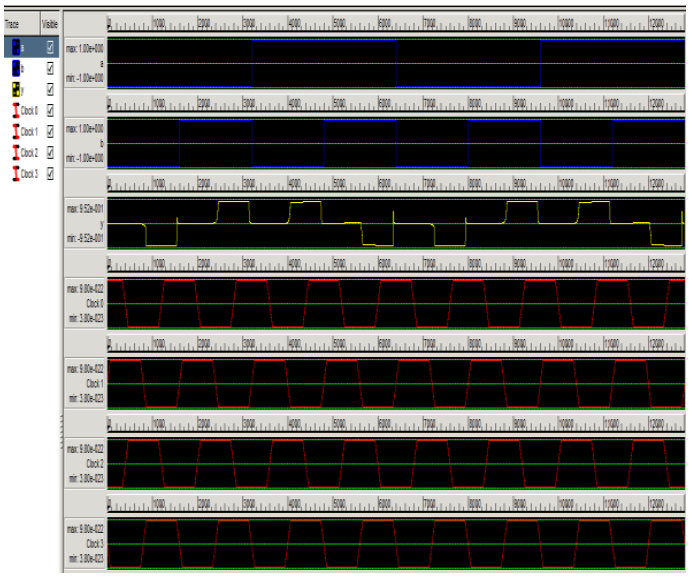

Fig. 13 Simulated output of XOR

The output of binary to gray code convertor is shown in below fig.

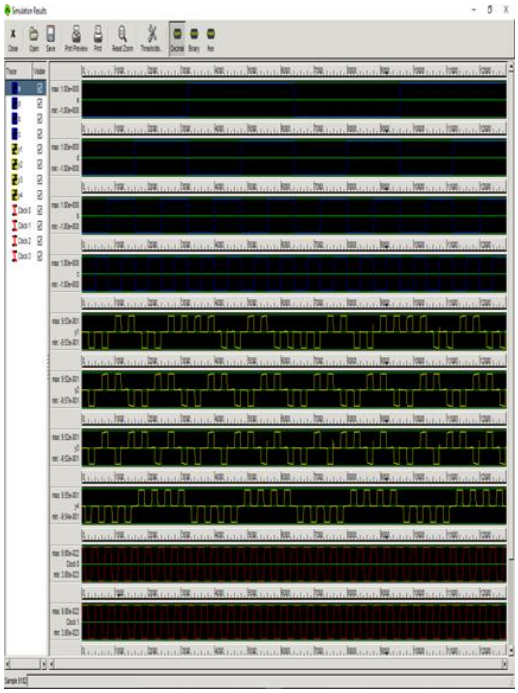

Fig.14 Simulated output of binary to gray code converter

Similarly the simulation output of gray to binary code convertor is also shown below

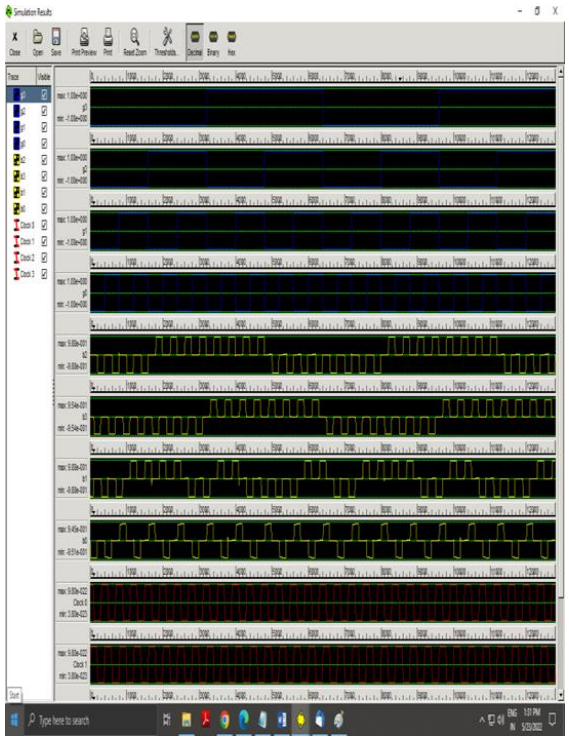

Fig. 15 Simulated output of gray to binary code converter

II. CONCLUSION

Table 5

	Existing Cell count	Proposed cell count
XOR	13	8
Binary to Gray	50	25
Gray to Binary	60	28

In this paper, an area efficient XOR gate is designed which is used to implement an effective design of Binary to Gray code and gray to binary code converter. An extensive comparison has been carried out for all the proposed designs with the previous designs. It can be noticed that, the designs outperformed the previous design in metrics like area as well as cell count. The proposed designs were designed and simulated using QCA Designer tool.

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