International Journal of Scientific Research in Science and Technology
Print ISSN: 2395-6011 | Online ISSN: 2395-602X (www.ijsrst.com)
doi : https://doi.org/10.32628/IJSRST

Implementation Of Half Adder and Full Adder Using Cost Effective XOR Gate In QCA

[1]K. Lavanya, [2]O. Roothu, [3]N. Venkata Ramana, [4]M. Yogendar Reddy, [5]B. Druthyugna
[6]Smt. T. Ranjitha Devi
[1,2,3,4,5]B. Tech Scholar, [6]Assistant Professor
Department of ECE, SVIT, Ananthapuramu, Andhra Pradesh, India

Article Info
Volume 9, Issue 3
Page Number : 675-681
Publication Issue
May-June-2022
Article History
Accepted : 10 June 2022
Published : 20 June 2022

ABSTRACT

In this project, we proposed a proficient, low complex 2-bit QCA XOR gate has been suggested. By using the proposed XOR and half adder and full adder is designed. Quantum-dot cellular automata (QCA) is an inventive Nano level computation that suggests less dimension, less power consumption, with more speed and premeditated as an amplification to the scaling obstacle with CMOS methodology. One of the newest and rising nanotechnologies used today is QCA based on the repulsion of Coulomb. One of the newest and rising nanotechnologies used today is QCA based on the repulsion of Coulomb. Surmised computing is a successful paradigm for energy efficient hardware design in Nano-scale. Further the suggested QCA XOR gates are utilized to design half adder and full adder using QCA Designer tool. The proposed QCA XOR gate contains very less number of quantum cells as well as areas such that half adder also possess same characteristics compared to existing QCA layouts. The simulation outcomes illustrate that the promised structure diminishes the number of cells, area utilized to make the design cost effective. The proposed QCA XOR gate, half adder and full adder contains very less number of quantum cells as well as areas as related to its best previous existing QCA layouts. These implemented designed are simulated and waveforms are observed using QCA designer tool.

Keywords: Quantum dot cellular automata (QCA), XOR, half adder, full adder, QCA Designer, majority gate, electrons, CMOS (complemented metal oxide semiconductor)

I. INTRODUCTION

QCA (Quantum-dot Cellular Automata) is one of the most attractive alternatives for CMOS technology. QCA uses the paired order of quantum dots to implement the Boolean logic functions. QCA is physical implementation of a classic cellular automata from mechanic quantum effect.

The common digital technologies use the voltage or current ranges for showing the logic values, whilst in

QCA technology, the situation of electrons in quantum dots shows the binary values.

The advantages of this technology include:

1. High operational speed (Tera Hertz range),
2. Low power consumption (approximately 100),
3. High device density.

Minimum feature in CMOS has reduced after several decades, however, facing some limitation. This subject caused the rapid development of molecular plans in Nano-scale. QCA is a hopeful sample in nanotechnology, suggested by Lent et al. and created in 1997.

According to the considerable features of QCA such as high density, low power consumption, high speed function potential and pipeline being advantage, QCA is changed as an interesting alternative technology for CMOS technology.

QCA is based upon encoding of binary information in the charge configuration within Quantum-dot cells. Computational power is provided by the Columbic interaction between QCA cells. No current flows between cells and no power or information is delivered to internal cells. The interconnection between QCA cells is provided by cell-to-cell interaction due to the rearrangement of electron positions .The two electrons are loaded in antipodal sides in Quantum-dots of a QCA cell.

A standard QCA cell is constituted of four quantum dots at four corners of a square cell. In this cell, four quantum dots have been paired together by the tunnel barriers. Two electrons existing in each cell may tunnel between the quantum dots inside the cell.

The high intercellular potential barriers ensure that no electron tunnels between QCA cells. Figure below shows a standard QCA cell with four quantum dots located at its corners.

The efficacy of columbic interaction have run two electrons each to the cell diameters. The polarization of both stable states in cell diameters provides binary logic 0 and binary logic 1.

Figure exhibits the state of electrons placed in cell diameters and 0 and 1 binary information. If two cells are located next to each other, the columbic interaction between the electrons causes the cells to have equal polarization and the same value of its left side cell.

In fig. some of QCA cells have been located beside each other and formed a wire in QCA. In QCA technique, the wires are 45 and 90 degrees. Both wire types are used in the cross over and arrays intensively.

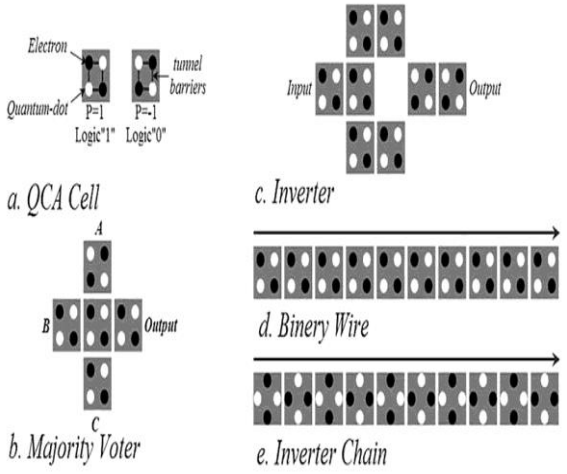


Fig. 1 a) QCA cell b) Majority Voter c) Inverter d) Binary Wire e) Inverted Chain

QCA clocking has been performed through timing in four distinct phases and required for both combinational and sequential circuits. Clocking not only controls the data current but provides the actual power in QCA circuits. The clock used in QCA consists of 4 phases: Switch, Hold, Release and Relax.

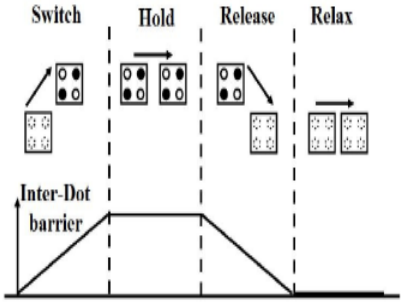


Fig. 2 QCA Clock Schemes

The signal energy lost by the medium is recovered by a new clocking. In QCA, clocking signals have been generated by an electrical field so that to control tunnel barriers in the quantum dots inside a QCA cell.

Quantum-dot cells are key components of QCA technologies to implement as Logic Gates, Wires, and Memories. The basic logic elements in QCA technology are the Majority gate and Inverter. Wires can be used for signal propagation in QCA circuits.

Logic elements such as AND gate & OR gate can be obtained by manipulating the Majority gate.

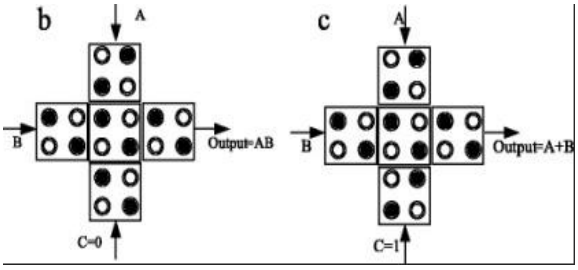
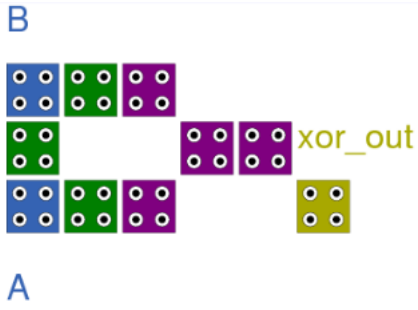


Fig. 3 AND & OR Gate

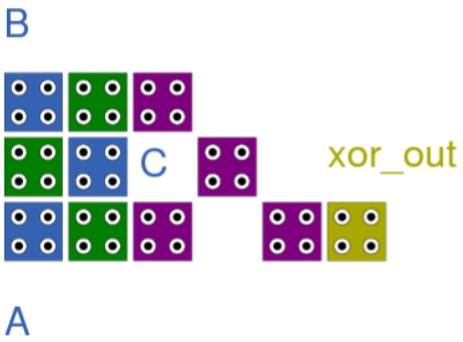
. Though the technology is different from convention CMOS designs, it is effective and realistic to implement the low power logic circuits. Thus, QCA is a new innovation at Nano-scale and an appealing substitute to ordinary CMOS. It is a possible technology for the next generation of digital circuits and systems and widely utilized as a part of advanced frameworks.

II. EARLIER WORK

An EX-OR gate is a very common gate used in ICs and ALU. It is vital while designing any compound circuits. In earlier design, various XOR gates have been created in QCA designer.

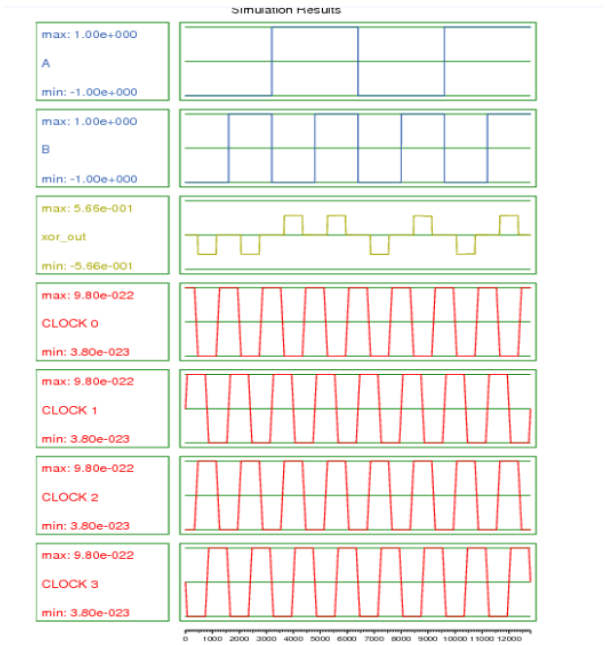


(a)



(b)

Fig. 4 (a)2-input XOR (b)3-input XOR



(a)

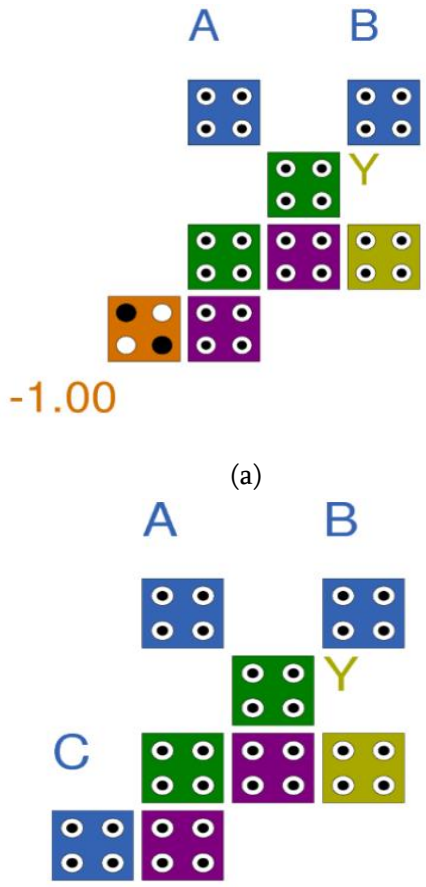
(b)

Fig. 5 Simulated Output waveform of (a) 2-input XOR (b) 3-input XOR

As from the output waveform we can conclude that the earlier design is having delay of 1 clock which is a major drawback in the circuit.

III. PROPOSED WORK

In the proposed method, suggested QCA architectures 2 input XOR gate and its QCA layout is implemented. It consists of 8 QCA cells in which there are 2 inputs, one "-1" polarization and one output is there. In the existing design output delay is of 1 clock cycle and number of QCA cells are also more. The proposed 2-input & 3-input XOR gates are shown in the figure below.

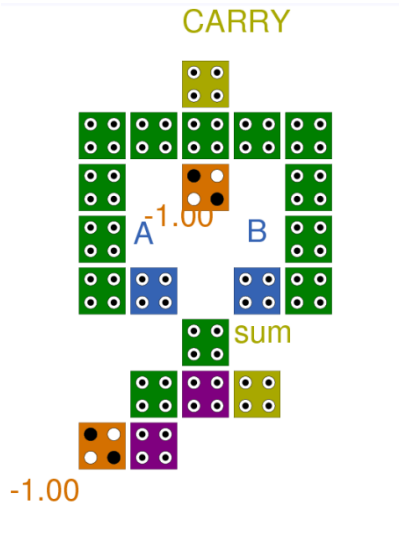


(a)

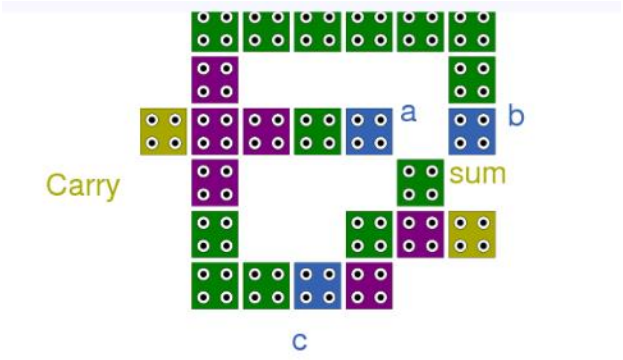
(b)

Fig. 6 (a) 2-input XOR (b) 3-input XOR

By using the 2-input & 3-input XOR gates half adder and full adder are designed respectively. Half adder and full adder are basic circuits which are used in most arithmetic operation for adding bits. The implementation of half adder and full adder using 2-input & 3-input XOR gates are shown below



(a)

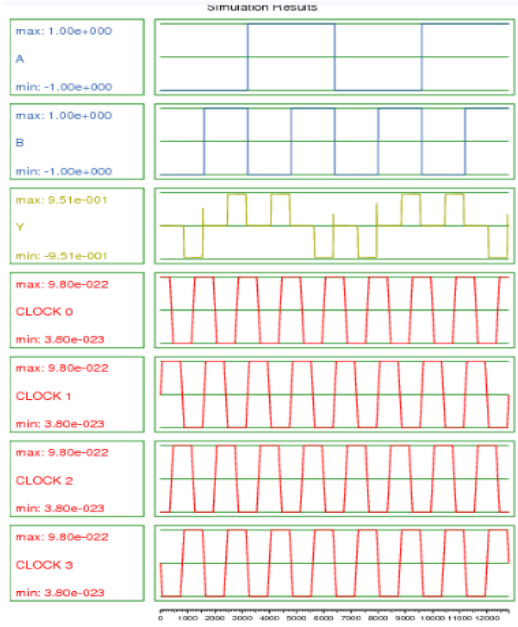


(b)

Fig. 7 (a) Half Adder (b) Full adder

IV. EXPERIMENTAL RESULTS

```
Starting Simulation
Total simulation time: 4 s
Simulation found 2 inputs 1 outputs 8 total cells
Starting initialization
Total initialization time: 0 s
Starting Simulation
Total simulation time: 3 s
```



(a)

```
Simulation found 3 inputs 1 outputs 8 total cells
Starting initialization
Total initialization time: 0 s
Starting Simulation
Total simulation time: 1 s
```

(b)

Fig. 8 Simulated Output of(a) 2-input XOR (b) 3-input XOR

```
File opened in 0.20 seconds
Simulation found 2 inputs 2 outputs 21 total cells
Starting initialization
Total initialization time: 1 s
Starting Simulation
Total simulation time: 4 s
```

(a)

(b)

Fig. 9 Simulated Output of (a) Half adder (b) Full adder

II. CONCLUSION

In this paper, an optimal way to execute a 2-input XOR gate is proposed. Using which a half adder as an application is also designed in the QCA Designer simulation tool for nanotechnology applications. According to execution parameter comparison, it is observed that the proposed half adder and full adder architectures buildup of ultra-efficient QCA XOR gate combinations to attain efficient and optimum layouts and achieved less parameter count like delay and area.

III. REFERENCES

[1]. 2013 International Technology Roadmap for Semiconductors (ITRS). 2013. Available online: https://www.semiconductors.org/ resources/2013-international-technology-roadmap-for-semiconductors-itrs/ (accessed on 3 August 2021).

[2]. Oya, T.; Asai, T.; Fukui, T.; Amemiya, Y. A majority-logic nanodevice using a balanced pair of single-electron boxes. J. Nanosci. Nanotechnol. 2002, 2, 333–342.

[3]. Oya, T.; Asai, T.; Fukui, T.; Amemiya, Y. A majority-logic device using an irreversible single-electron box. IEEE Trans. Nanotechnol. 2003, 2, 15–22.

[4]. Fahmy, H.A.H.; Kiehl, R.A. Complete logic family using tunneling-phase-logic devices. In Proceedings of the Eleventh International Conference on Microelectronics, ICM '99, Safat, Kuwait, 22–24 November 1999; pp. 153–156.

[5]. Zahoor, F.; Hussin, F.A.; Khanday, F.A.; Ahmad, M.R.; Mohd Nawi, I.; Ooi, C.Y.; Rokhani, F.Z. Carbon nanotube field effect transistor (cntfet) and resistive random access memory (rram) based ternary combinational logic circuits. Electronics 2021, 10, 79.

[6]. Tabrizchi, S.; Panahi, A.; Sharifi, F.; Mahmoodi, H.; Badawy, A.H.A. Energy-Efficient Ternary Multipliers Using CNT Transistors. Electronics 2020, 9, 643.

[7]. Lent, C.S.; Tougaw, P.D.; Porod, W.; Bernstein, G.H. Quantum cellular automata. Nanotechnology 1993, 4, 49.

[8]. Tougaw, P.D.; Lent, C.S. Logical devices implemented using quantum cellular automata. J. Appl. Phys. 1994, 75, 1818–1825.

[9]. Lent, C.S.; Tougaw, P.D. A device architecture for computing with quantum dots. Proc. IEEE 1997, 85, 541–557.

[10]. Porod, W. Quantum-dot devices and quantum-dot cellular automata. Intern. J. Bifurc. Chaos 1997, 7, 2199–2218.

[11]. Snider, G.; Orlov, A.; Amlani, I.; Zuo, X.; Bernstein, G.; Lent, C.; Merz, J.; Porod, W. Quantum-dot cellular automata: Review and recent experiments. J. Appl. Phys. 1999, 85, 4283–4285.

[12]. Walus, K.; Jullien, G.A.; Dimitrov, V.S. Computer arithmetic structures for quantum cellular automata. In Proceedings of the Conference Record of the Thirty-Seventh Asilomar Conference on Signals, Systems & Computers, Pacific Grove, CA, USA, 9–12 November 2003; Volume 2, pp. 1435–1439.

[13]. AlKaldy, E.; Majeed, A.H.; Zainal, M.S.; Nor, D.M. Optimum multiplexer design in quantum-dot cellular automata. arXiv 2020, arXiv:2002.00360.

[14]. Sabbaghi-Nadooshan, R.; Kianpour, M. A novel QCA implementation of MUX-based universal shift register. J. Comput. Electron. 2014, 13, 198–210.

[15]. Sen, B.; Dutta, M.; Goswami, M.; Sikdar, B.K. Modular design of testable reversible ALU by QCA multiplexer with increase in programmability. Microelectron. J. 2014, 45, 1522–1532.

[16]. Rashidi, H.; Rezai, A.; Soltany, S. High-performance multiplexer architecture for quantum-dot cellular automata. J. Comput. Electron. 2016, 15, 968–981.

[17]. Asfestani, M.N.; Heikalabad, S.R. A unique structure for the multiplexer in quantum-dot cellular automata to create a revolution in design of nanostructures. Phys. B Condens. Matter 2017, 512, 91–99.

[18]. Song, Z.; Xie, G.; Cheng, X.; Wang, L.; Zhang, Y. An Ultra-Low Cost Multilayer RAM in Quantum-Dot Cellular Automata. IEEE Trans. Circuits Syst. II 2020, 67, 3397–3401.

[19]. Bahar, A.N.; Wahid, K.A. Design and Implementation of Approximate DCT Architecture in Quantum-Dot Cellular Automata. IEEE Trans. VLSI Syst. 2020, 28, 2530–2539.

[20]. Sen, B.; Goswami, M.; Mazumdar, S.; Sikdar, B.K. Towards modular design of reliable quantum-dot cellular automata logic circuit using multiplexers. Comput. Electr. Eng. 2015, 45, 42–54.

[21]. Sen, B.; Dutta, M.; Saran, D.; Sikdar, B.K. An efficient multiplexer in quantum-dot cellular automata. In Progress in VLSI Design and Test; Springer: Berlin/Heidelberg, Germany, 2012; pp. 350–351.

[22]. Raj, M.; Gopalakrishnan, L.; Ko, S.B.; Naganathan, N.; Ramasubramanian, N. Configurable Logic Blocks and Memory Blocks for Beyond-CMOS FPGA-Based Embedded Systems. IEEE Embed. Syst. Lett. 2020, 12, 113–116.

[23]. Wang, L.; Xie, G. A Novel XOR/XNOR Structure for Modular Design of QCA Circuits. IEEE Trans. Circuits Syst. II 2020, 67, 3327–3331.

Cite this article as :

K. Lavanya, O. Roothu, N. Venkata Ramana, M. Yogendar Reddy, B. Druthyugna, Smt. T. Ranjitha Devi, "Implementation Of Half Adder and Full Adder Using Cost Effective XOR Gate In QCA", International Journal of Scientific Research in Science and Technology (IJSRST), Online ISSN : 2395-602X, Print ISSN : 2395-6011, Volume 9 Issue 3, pp. 675-681, May-June 2022.
Journal URL : https://ijsrst.com/IJSRST22293139