International Journal of Scientific Research in Science and Technology
Print ISSN: 2395-6011 | Online ISSN: 2395-602X (www.ijsrst.com)
doi : https://doi.org/10.32628/IJSRST

Design of High-Performance Flash ADC Using Domino Logic

Keerti Sangappa
M. Tech Scholar, Department of ECE (VLSI & EMBEDDED SYSTEM), Sharnbasva University, Kalaburagi, India

Article Info
Volume 9, Issue 4
Page Number : 266-271

Publication Issue
July-August 2022

Article History
Accepted : 05 July 2022
Published : 20 July 2022

ABSTRACT

In this paper, Flash Analog to digital converter is implemented. The designed Flash ADC consists of a resistive ladder network, comparators, the thermometer to a binary encoder and the entire design is carried out using Tanner tools employing 180nm technology. The reference voltage applied to the resistive ladder network is 1.8V. A two-stage operational amplifier is used as a comparator in the flash ADC. Binary code is obtained from the thermometer code by utilizing a priority encoder. The major problem that usually appears in flash ADC is as the number of resolution bits increases, the Area, as well as the power consumption of the circuit, also increases. In this paper, we principally concentrated to lessen the propagation delay of the ADC by optimizing encoder circuitry. With the purpose of reducing latency, Encoder is implemented using 2:1 mux based on domino logic. Performance parameters of Flash ADC such as delay as well as average power are calculated and compared.

Keywords: Flash ADC, Domino Logic, Mux Based Encoder.

I. INTRODUCTION

Digital signal processing has advanced intensely due to the rapid expansion of science and technology. In the majority of the digital domains, signal processing offers several advantages such as flexibility in design and programmability, reduced silicon area, high accuracy, as well as a smaller amount of power consumption. The design process is cost-effective and faster. Hence it is possible to design a system with a lesser area along with high speed. It is required to have an analog to digital converter that offers much higher speed in wireless communication, image processing, etc. [1]

In last few years the largest portion of electronics industry is dominated by MOS market. It becomes a challenging to design analog circuit reducing its feature sizes, supply voltages as well as transistor channel length. Op amp can easily trade-off between all performance parameters like gain, phase, phase margin, unity gain bandwidth etc. The design can be achieved handling various aspect ratios i.e changing width and length of transistors to be in saturation region so that it can give better performance. It is preferred to have digital systems that are portable and have prolonged battery life. This can be only possible by developing applications that consume less power. Since ADC s act as front-end components in the majority of mixed-signal systems, we focused to

design ADC that consumes less power which in turn offers higher speed. We have various types of ADC architectures for instance successive approximation type ADC, Flash type, sigma-delta, etc. Among these Flash ADC is preferred since it offers high speed because of its parallel architecture, the conversion time is not limited by resolution hence these ADC s are utilized in those systems where bandwidth with a wide range and high speed is required[2].

Mirza Nemeth Ali Baig and Rakesh Ranjan have implemented high-speed flash ADC for wireless LAN applications. Seven operational transconductance-based comparators with a reference voltage of 250mV are used to construct the planned 3-bit flash Analog to digital converter, and complete adders are used to perform the high-speed encoder. Since ADC is implemented by utilizing a full adder based encoder, the area is limited by the resolution[5]. Sarojini Mandal and J.K.das had implemented a 3-bit flash ADC using cascading full adder by using pass transistor logic that makes the circuit much faster. They have improved the efficiency of flash ADC by improving the working of the comparator by scaling down the length to width ratio of transistors assuming transistors operating in the saturation region. A complete adder with ten transistors is used to create the encoder circuit. The use of pass transistor logic in a complete adder circuit reduces the chip s complexity and space. Logic levels will worsen since the entire adder is constructed with a pass transistor [6].

Domino Logic:

Domino logic family find a wide variety of application, where less transistor count and high speed of operation such as microprocessor, dynamic memory, digital signal processors etc are required. Domino logic is an evolution in CMOS based dynamic logic techniques which use either p-MOS or n-MOS for the pull down or pull up network. The methodology of designing full adder by using Domino logic employs lesser no. of transistors as if compared to conventional CMOS logic and provides high performance device.

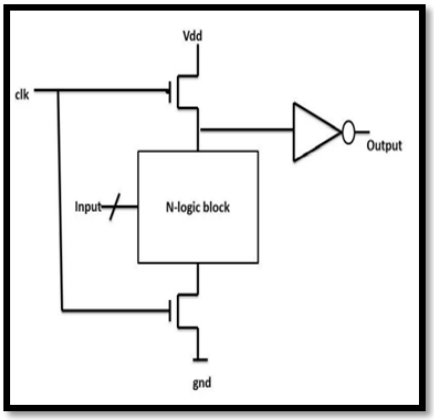

Figure 1: Block diagram of Domino Logic

II. EARLIER WORK

To implement N bit flash ADC, we require 2N-1 comparators are needed. Similar to op-amp, the comparator comprises of two inputs where analog input is given to the inverting terminal and reference voltage is applied to non-inverting terminal. Comparators are divided with the help of the resistive ladder network. 2N resistors are utilized to form a resistive ladder network of N bit. Since we have implemented 3-bit, the number of resistors required will be eight. The reference voltage is generated across the resistive ladder network between reference voltage and ground is equally distributed and is differed by the least significant bit. The comparator compares the reference voltage signal with the input analog signal and indicates output as logic high whenever analog input exceeds reference voltage and indicates logic low output when analog input is smaller than reference voltage. The output of comparators forms a thermometer code. Further, we need to translate thermometer code into binary code.

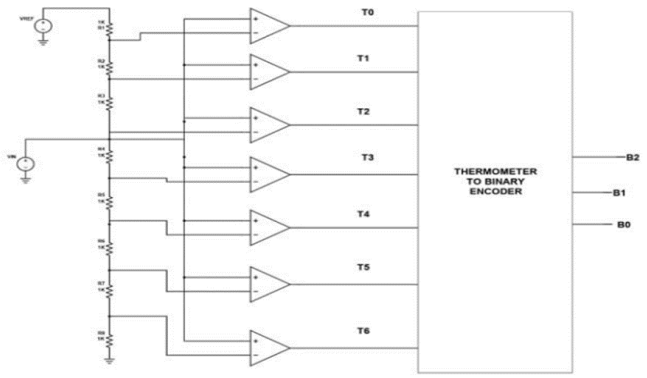

Figure 2: Circuit of Flash ADC

Operational amplifier as a comparator:

The applied input signal is compared with the reference signal and will provide output as shown below.

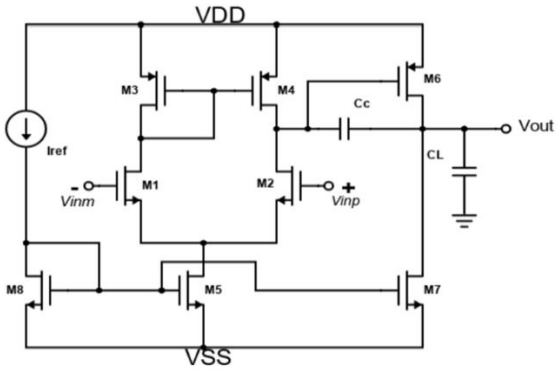

Figure 3: Block diagram of Two stage Op-Amp

The above fig.3 shows a block diagram of the two-stage op-amp. It consists of a differential voltage gain stage followed by a common source gain stage. Differential inputs are applied through the M1 transistor along with the M2 transistor. Op-amp Biasing is furnished with the transistors M5 and M8 to ensure all transistors in saturation. The current mirror formed by the transistor M3 and M4 mirrors current from transistor M1 and is subtracted from the transistor M2. If sufficient gain is not obtained during the differential stage then we use a common source amplifier as the gain stage which is formed by transistors M6 and M7.

Thermometer to binary code encoder design:

Thermometer code can be translated to binary code in different ways. The name thermometer code is given because the output of the comparators looks like thermometer reading that is as the value increases the number of ones goes on increasing same like the mercury level which increases as temperature increases. There are different types of encoders to convert thermometer code into binary code for instance Wallace tree encoder, encoder design utilizing mux, and encoder using xor as well as ROM encoder. Each of these encoders has its own advantages and disadvantages. Encoder designed using Mux operates on the simple logic that is if half of the thermometer code represents logic high the most significant bit in binary code is also high. The value corresponding to 2n-1 represents MSB in the binary output. Again this thermometer code is classified into two codes to find next binary output. A select line of the second stage Mux is obtained from the preceding stage mux output. The procedure is continued till the end of the last 2:1 mux and the least significant bit of binary output is obtained. Even if resolution increases we can implement an encoder using this 2:1 mux easily with less area and less power consumption.

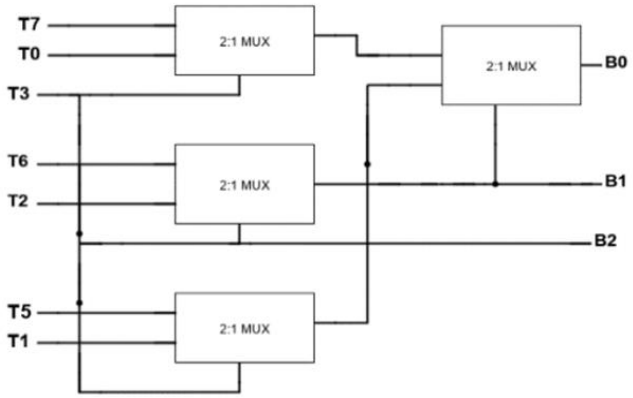

Figure 4 Encoder Implementation using 2:1 MUX

Here, the MUX is designed with Transmission gates instead of Pass Transistor Logic and CMOS Logic.

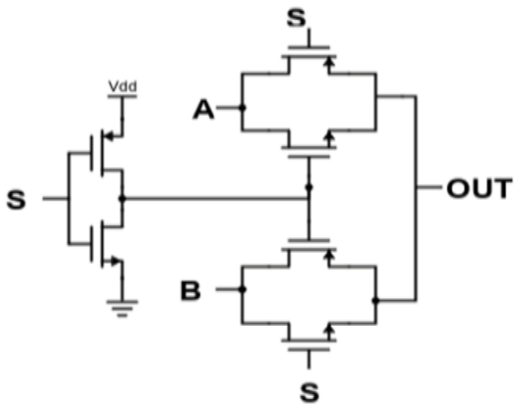

Figure 5: Mux using Transmission Gate (Switch Logic)
Due to the implementation of mux using CMOS transmission gate, the number of transistors got reduced which reduced the power consumption, area and increases speed.

III. PROPOSED WORK

The Domino logic is an improvement in dynamic logic which has a drawback when one gate is cascaded to next. In domino logic, A static inverter is used between the two stages for removing the drawback of dynamic logic. There are various advantages of Domino logic like they have a smaller area unlike conventional CMOS logic, parasitic capacitance are smaller in domino logic so it provide high speed of operation and result is glitch free because each gate makes only one transition. Domino logic style is generally used for designing a high performance circuit, rather than a static logic style. For arithmetic operations full adder acts as a basic element for parity checker, comparator and multiplier, hence it receives a lot of attention by the researchers.

Domino logic consists of two- stages of operation in which first stage is pre-charging, and another stage is evaluation. As shown in fig.1, when clock clk is equal to zero or low pMOS will be on and it pre-charged the output node to Vdd. When the clk goes to high, p-MOS will be off and the evaluation phase will start. In this phase output will depend on the input s configuration. Output node may discharge if inputs have a direct conducting path to ground otherwise it will remain high. So the output of circuit is obtained by which it has been intended to design in evaluation phase only. In pre-charge phase, it will provide low output because we used an inverter in this logic style for cascading the next stage.

MUX using Domino Logic:

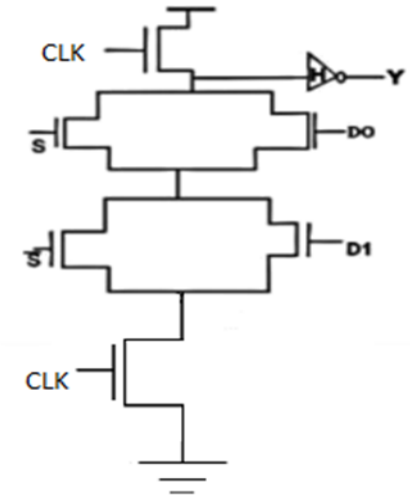

Figure 6: Schematics of MUX using Domino logic

IV. EXPERIMENTAL RESULTS

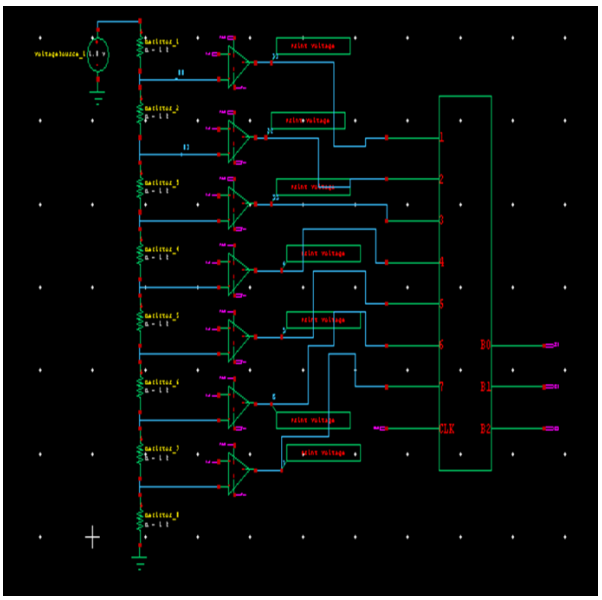

Figure 7: Schematic of proposed Flash ADC

Figure 7 shows Tanner tool diagram of suggested Flash ADC employing MUX based encoder in which MUX is designed using Domino Logic.

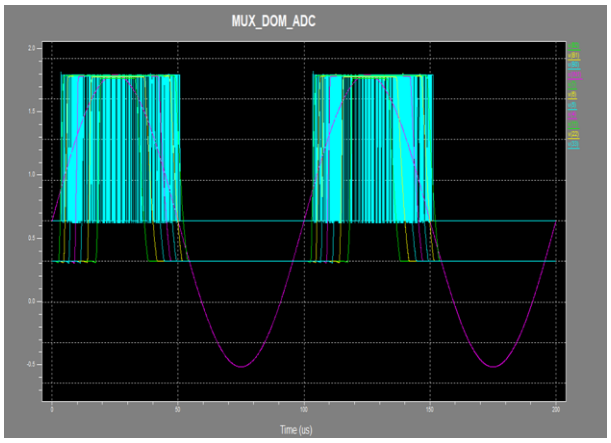

Fig 8: Simulation results for proposed Flash ADC

Figure 8 shows the results of waveforms for recommended Flash ADC using Domino logic oriented MUX.

	CMOS MUX	PTL MUX	SL MUX	DOMINO MUX
Power ((10-4W)	1.942	1.941	1.9538	1.942
Area	108	68	84	96
Delay	8.976µs	8.689µs	0.4µs	2.613µs

Table 1 : comparison of Flash ADC between different MUX based encoders.

Table1 describes the comparison of performance parameters such as Area, Delay and Power between MUX based encoders for Flash ADC.

From these results, we conclude that the power dissipation and area is reduced PTL MUX but the delay is more. The delay is less in SL MUX but power dissipation is more. In DOMINO MUX, the power is approximately similar to CMOS MUX whereas the area is more compared to PTL and SL based MUX, the delay is less compared to CMOS as well as PTL based MUX.

On comparing Flash ADC, with all these MUX based encoder, it is proven that the Domino Logic MUX based encoder utilizing Flash ADC has achieved better overall performance than the other Flash ADC.

V. CONCLUSION

We used domino logic in this paper to construct flash ADC. The Tanner tool, which uses 180nm technology model files, is used to design and simulate a 3-bit flash ADC. The average power of a 3-bit flash ADC is determined and compared. By modifying the encoder circuitry, we were able to reduce the propagation latency of the 3-bit flash ADC. We used domino logic to construct a 2:1 mux encoder. Less delay is achieved by using a 3-bit Flash ADC with a 2:1 mux in Domino Logic.

VI. REFERENCES

[1]. Glyny George, A. V. Jos Prakash, Design of ultra-low voltage high speed flash ADC in 45nm CMOS Technology, IEEE Conference on recent trends in electronics, Information &communication technology, 2018.

[2]. S. Veeramachanen, A. M. Kumar, V. Tummala and M. B. Srinivas, Design of a Low Power, Variable-Resolution Flash ADC, 2009 22nd International Conference on VLSI Design, New Delhi, 2009

[3]. Al-Ahsan Talukder, Md. ShamimSarker, A three-bit threshold inverter quantization based CMOS flash ADC , 2017 4th International Conference on Advances in Electrical Engineering, 2017.

[4]. Sonu Kumar, Anjali Sharma, Design of CMOS operational amplifier in 180nm technology , International journal of innovative research in computer and communication engineering Vol.5, issue 4, April 2017.

[5]. MirzaNemath Ali Baig, RakeshRanjan, Design and implementation of 3-bit High-speed flash

ADC for wireless LAN Applications, IJARCCE, Vol 6, 2017.

[6]. SarojiniMandal, Dr. J.K Das, Design of 3-bit low power flash ADC, IJARCET, Volume 3 issue 4, April 2014.

[7]. Jayesh J. Vyas, Simulation of 3 bit Flash ADC in 0.18um technology using Ngspice Tool for High-speed applications, IJSRD, volume 1, Issue 2, 2013.

[8]. Piyush. V. Kanodiya, Amisha. P. Naik, Analysis and design of flash Analog to digital converter for ultra-wideband applications, IEEE 2011.

[9]. Pradeep Kumar, AmitKolhe, Design & Implementation of Low Power 3-bit Flash ADC in 0.18μm CMOS, International Journal of Soft Computing and Engineering (IJSCE), ISSN: 2231-2307, Volume-1, Issue-5, November 2015.

[10]. Ashima Gupta, anil Singh, Highly digital voltage scalable 4-bit flash ADC, IET circuits, devices &systems, 2019.

Cite this article as :

Keerti Sangappa, "Design of High-Performance Flash ADC Using Domino Logic", International Journal of Scientific Research in Science and Technology (IJSRST), Online ISSN : 2395-602X, Print ISSN : 2395-6011, Volume 9 Issue 4, pp. 266-271, July-August 2022.
Journal URL : https://ijsrst.com/IJSRST229442