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A Novel Design of Full Adder Using Efficient Mux In QCA

Vasia Ibtasaum[1], Dr. Anuradha Savadi[2]

[1]M.Tech Scholar, Department of ECE (VLSI & EMBEDDED SYSTEM), Sharnbasva University, Kalaburagi, India

[2]Associate Professor Department of ECE, Sharnbasva University, Kalaburagi, India

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ABSTRACT

In this project, the MUX design is modified and proposed in QCA. QCA technology is expected to be a feasible alternative to CMOS circuit implementation in terms of energy efficiency, integration density, and switching frequency as nm technology decreases. For developing QCA circuits, MUX (Multiplexer) is seen to be a good choice. With approximate reductions in area, the suggested complete adder outperforms the best current design. In addition, as compared to existing architectures, same or higher performance characteristics like power and latency are obtained. The suggested design has an outstanding scaling feature and may be utilized to create energy-efficient complicated QCA circuits. These implemented designed are simulated and waveforms are observed in QCA Designer tool.

Keywords: MUX (Multiplexer), QCA, CMOS, QCA Designer tool

I. INTRODUCTION

In CMOS technology VLSI served as an effective way for implementing circuits. Also researches have been carried out to develop next step of this technology out of which QCA (Quantum-dot Cellular Automata) is considered as a better substitution of CMOS technology. In QCA technology there is a paired order of quantum dots which performs any Boolean functions. QCA is nothing but a real time development of cellular automation from quantum mechanics.

In general digital system uses voltage or current ranges as the logic values where in Quantum Dot Cellular Automata, the electrons positions in quantum dots determines the binary values.

Pros of QCA:

1. High operational speed (Tera Hertz range),
2. Low power consumption (approximately 100),
3. High device density.

Minimum feature in CMOS has reduced after several decades, however, facing some limitation. This subject caused the rapid development of molecular plans in Nano-scale. QCA is a hopeful sample in nanotechnology, suggested by Lent et al. and created in 1997.

According to the considerable features of QCA such as high density, low power consumption, high speed function potential and pipeline being advantage, QCA is changed as an interesting alternative technology for CMOS technology.

Quantum-dot cells are used in QCA to encode binary information in the charge configuration. The Columbic contact between QCA cells provides computational strength. Internal cells get no power or information since there is no current flowing between them. Cell-to-cell contact, which is caused by the rearranging of electron locations, provides connectivity between QCA cells. In Quantum-dots of a QCA cell, the two electrons are loaded on opposite sides.

In a QCA cell four quantum dots are placed at the corner of a square cell. There is a link among those quantum dots which is called tunnel barriers in the QCA cell. There are two electrons in every cell which can tunnel between those quantum dots.

No electron tunnels exist between QCA cells due to the large intercellular potential barriers. A conventional QCA cell with four quantum dots at its corners is seen in the illustration.

The efficacy of columbic interaction have run two electrons each to the cell diameters. The polarization of both stable states in cell diameters provides binary logic 0 and binary logic 1.

Figure exhibits the state of electrons placed in cell diameters and 0 and 1 binary information. If two cells are located next to each other, the columbic interaction between the electrons causes the cells to have equal polarization and the same value of its left side cell.

In Fig. some of QCA cells have been located beside each other and formed a wire in QCA. In QCA technique, the wires are 45 and 90 degrees. Both wire types are used in the cross over and arrays intensively.

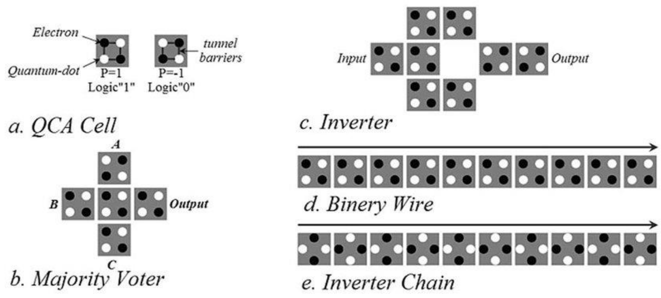


Fig. 1 a) QCA cell b) Majority Voter c) Inverter d) Binary Wire e) Inverted Chain

QCA clocking has been performed through timing in four distinct phases and required for both combinational and sequential circuits. Clocking not only controls the data current but provides the actual power in QCA circuits. The clock used in QCA consists of 4 phases: Switch, Hold, Release and Relax.

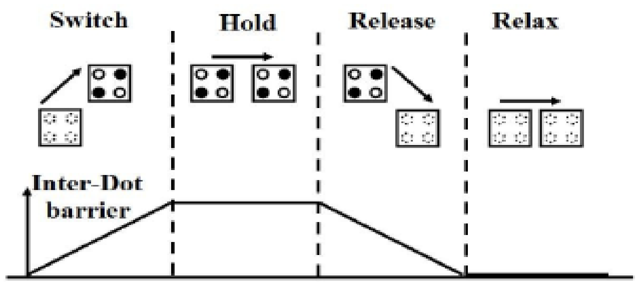


Fig. 2 QCA Clock Schemes

The signal energy lost by the medium is recovered by a new clocking. In QCA, clocking signals have been generated by an electrical field so that to control tunnel barriers in the quantum dots inside a QCA cell. Quantum-dot cells, which may be used as Logic Gates, Wires, and Memories, are essential components of QCA technologies. In QCA technology Majority voter gate and Inverter are the two fundamental gates used. For signal propagation wires are used, which is nothing but an array of QCA cells.

For implementing AND and OR gates a majority voter gate can be employed.

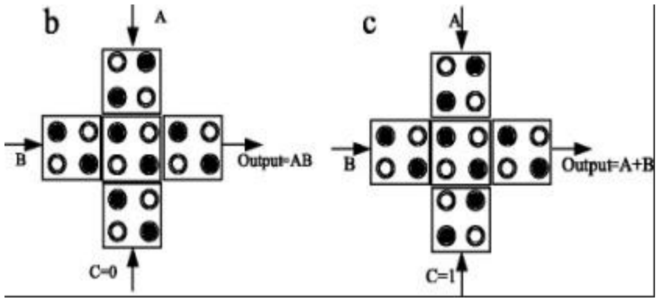


Fig. 3 AND & OR Gate

Despite the fact that the technology is not the same as traditional CMOS designs, the low-power logic circuits are practical and feasible to execute. As a result, QCA is a novel Nano-scale breakthrough and a viable alternative to conventional CMOS. It's a potential technology for future developments in circuits and systems.

II. PREVIOUS WORKS

As we know Multiplexer is considered as one of the fundamental functions used for implementing logic circuits. The 2 n × 1 MUX consists of 2 n inputs, n selector inputs, and 1 output. A 2 × 1 MUX performs the function given in Equation (1). $F = SI^{-}0 + SI1$ (1) In this paper, two different energy-efficient 2 × 1 MUX designs are proposed. These low-power designs are characterized by the relative positioning of the cells in the architecture. The first QCA structure of the proposed MUX is shown in Figure 1a. This is a square-like structure with three inputs (S, I1, I0), one constant, and one output (F). The constant is always set at logic 0, i.e., with a charge of –1.00. The input (I1) which is near the selector input (S) is the most significant bit in this 2 × 1 MUX. The input diagonally opposite to the selector is the least significant bit, which is I0 in this case. An alternate design is also possible by changing the constant to logic 1. In this case, the inputs I0 and I1 will interchange their positions which can be observed from the figure. The designs of existing 2 × 1 MUX with constant logic 0 and logic 1 are known as MUX1 and MUX2, respectively. The availability of MUX1 and MUX2 will give the options of selecting the best structure for designing different efficient-energy circuits.

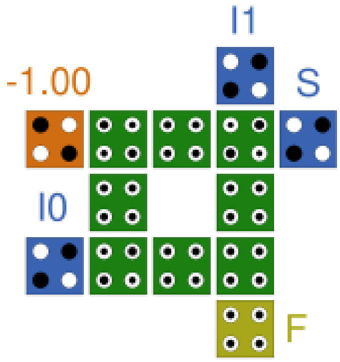


Fig. 4 Existing 2x1 MUX

Existing methods such as binary decision diagram (BDD) is used for implementing any logic functions using MUX. We know that a 4 × 1 MUX can be made using three 2 × 1 MUX. Similarly we can implement a 8 × 1 MUX using three 4 × 1 MUX, etc. Further simplification techniques are available for reducing total MUX used while implementation. A full adder circuit using MUX was designed

Block diagram for Full adder can be seen in figure 5

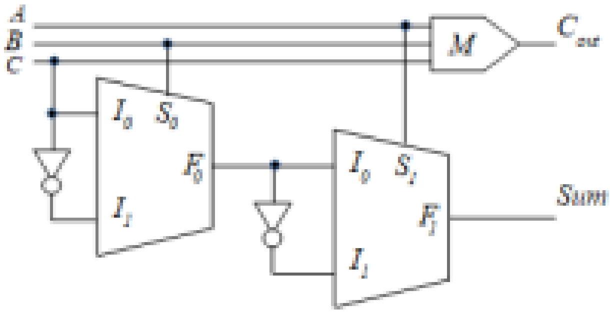


Fig. 5 Block Diagram

The Full adder design using MUX in QCA is given in figure 6.

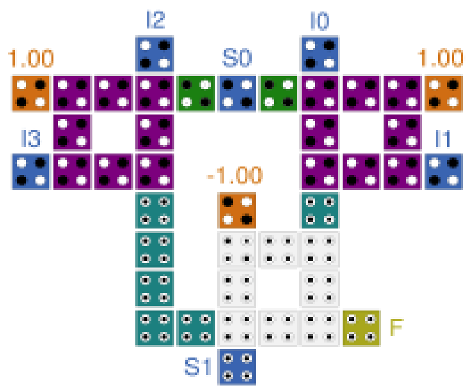


Fig. 6 Existing Full adder

We can observe from the figure that MUX1 is in the upper side, and MUX2 is in the lower side. The design is made is such that the result dissipates optimum energy. For first MUX clock 0 and clock 1 has been used. The outputs coming from the first stage MUX are given as inputs to second stage MUX, which are in clock zone 2. The final output is considered to be in clock zone 3. As a whole this style of clocking scheme found to have very less energy dissipation at the final stage.

III. PROPOSED WORK

In the proposed method, an improved way to implement full adder using mux is implemented in QCA technology. By comparing the previous suggested QCA architectures like 2:1MUX, 4:1MUX, from which full adder circuit is implemented. But the design is using more number of QCA cells which increases the total area consumption. On comparison the proposed design can be said to have improvement in parameter such as area making it as area efficient design.

A new design for full adder using efficient XOR gate in QCA is shown in fig. 7

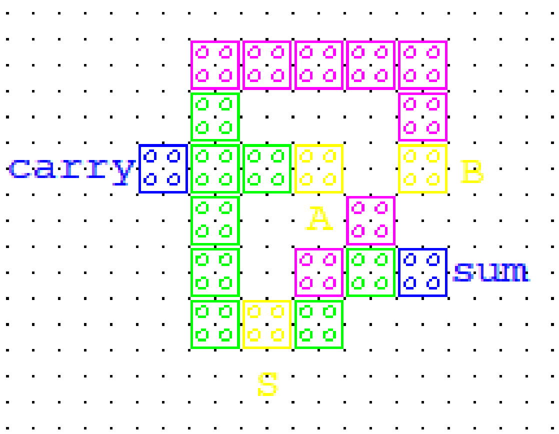
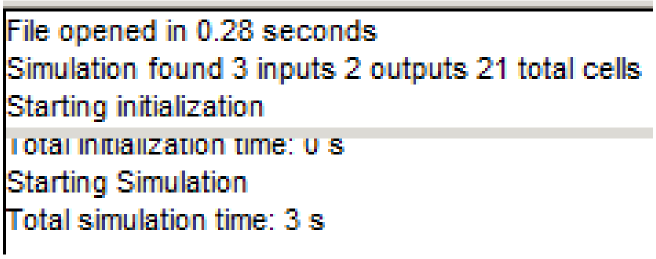


Fig. 7 Full adder

IV. SIMULATION RESULTS

Total cell count:



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Simulation found 3 inputs 2 outputs 21 total cells
Starting initialization
Total initialization time: 0 s
Starting Simulation
Total simulation time: 3 s

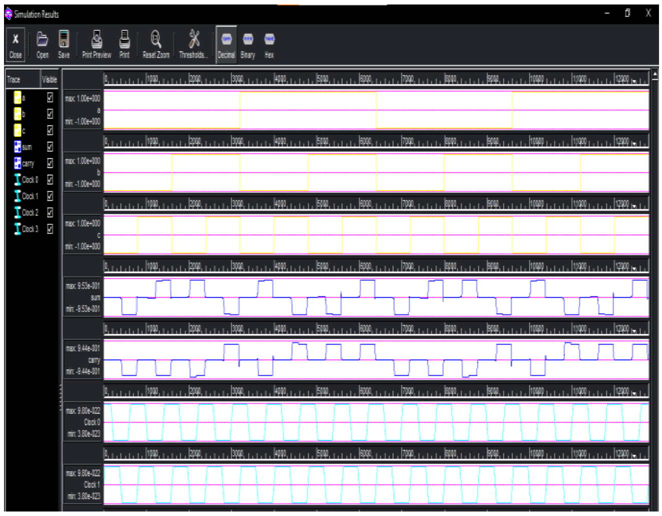

Fig. 7 Simulated output of Full adder

V. CONCLUSION

In this paper, an optimal way to execute a full adder using MUX in QCA is designed in the QCA Designer simulation tool for nanotechnology applications has been proposed. The morphological characteristics of this efficient design, ease highly dense circuitry execution. According to execution parameter comparison, it is observed that the proposed half adder architectures buildup of ultra-efficient full adder to attain efficient and optimum layouts and achieved less parameter count like area occupied.

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