International Journal of Scientific Research in Science and Technology
Print ISSN: 2395-6011 | Online ISSN: 2395-602X (www.ijsrst.com)
doi : https://doi.org/10.32628/IJSRST

Implementation of TSPC Flip-flop using Power Gating Technique

Triveni Jagadi[1], Vilaskumar Patil[2]
[1]PG Scholar, Department of ECE (VLSI & EMBEDDED SYSTEM), Sharnbasva University, Kalaburagi, India
[2]Associate Professor, Department of ECE, Sharnbasva University, Kalaburagi, India

Article Info
Volume 9, Issue 4
Page Number : 361-366
Publication Issue
July-August 2022
Article History
Accepted : 10 July 2022
Published : 26 July 2022

ABSTRACT

Power optimization is a very crucial issue in low voltage applications. This paper presents a design of D-Flip-Flop circuit using header power gating technique for low power operation. The primary goal of the design is to examine the power dissipation of D Flip-Flop in the proposed design style. The proposed design is implemented in Tanner EDA. The simulation results show that there is a significant reduction in power consumption for the proposed cell with power gating.

Keywords : Power gating, D Flip-flop, Low voltage applications, TSPC.

I. INTRODUCTION

Mostly in design of integrated circuits, power consumption is a crucial concern. Large heat dissipation has a negative impact on performance and dependability. Another reason to limit power dissipation is to make the battery last longer. Digital circuitry makes extensive use of D flip-flops. Its power dissipation is minimized, resulting in a significant reduction in overall power consumption.

The rising market for portable, battery-powered electronic systems (such as cellular phones and personal digital assistants) necessitates the development of low-power microelectronic circuits. The difficulty of delivering power dissipation may limit the functionality of computing systems as the density and complexity of processors continues to expand. Power dissipation, in particular, consumes around 35% of the chip's power at the nanoscale level. The goal of this research is to examine the performance of Power Gating, which is one of the most reliable ways to low-power design. The emphasis is solely on nanometer-scale CMOS devices, as this is the most widely used technology in today's VLSI systems. A circuit can function in two modes when using the power gating arrangement. Sleep transistors can be employed as functional redundant resistances when they are triggered in the active state. To decrease leakage power, the sleep transistors are turned off in sleep mode. A sleep transistor is known as a Header switch when it is connected to supply voltage, and as a Footer switch when it is connected to ground. The header power gating approach was employed in this project.

Flip-flops are crucial building blocks of sequential digital circuits, but they typically take up a large amount of chip space and require a lot of power. Flip-

flops are the basic building components of a sequential digital circuit. Because they have two stable states, logic low and logic high, flip-flops are also known as bistable circuits. Any triggering sets the circuit in one state, and any triggering change causes the flip-flop to switch states, necessitating the usage of a trigger pulse to change the state. In addition, clock signals are used as control inputs in Flip-Flops. One bit is stored in each flip-flop.

D Flip-Flop is represented by the block diagram below.

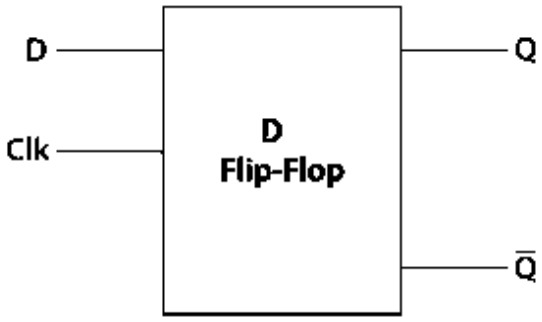

Fig.1: D Flip-Flop Block Diagram

D Flip-Flops are also found in data processors and memory storage elements. A D flip-flop can be built using either the NAND or the NOR gates. Because of their versatility, they are accessible as IC packages. A D Flip-Flop functions include adding delay to a timing circuit, acting as a buffer, and sampling data at predefined intervals. D flip-flops feature a more straightforward electrical connection than JK flip-flops.

The input state has no influence on the output state when the clock signal is in logic low level. In order for the inputs to become active, the clock must be set to a high value. hence the D Flip-Flop operates as a controlled Bi-stable latch, with the clock signal acting as the control input. Positive edge triggered D flip flops and negative edge triggered D flip flops are the two types of D Flip-Flop. As a consequence, the output has two stable states depending on the inputs.

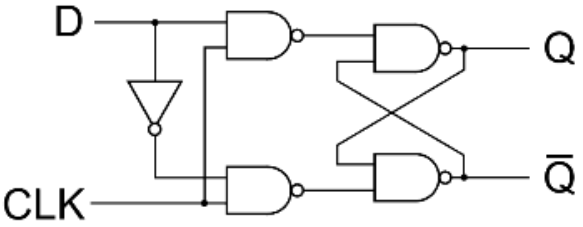

Fig.2 :Conventional gate level architecture of D Flip-Flop

Table 1: D Flip-Flop truth table

Clock	D	Q	qb
0	0	Q	qb
0	1	Q	qb
1	0	0	1
1	1	1	0

From the above truth table, it can be observed that when the clock signal is high only, the data present in d input will be transferred to q output.

Since the performance of Flip-Flops impacts the application, it is necessary to improve the performance of Flip-Flop.

II. RELATED WORKS

A static single-phase-clocked contention-free FF (S2CFF) is proposed in this method. Since conventional TSPC FF is based on dynamic logic and the voltage of internal nodes is not retentive, it is not suitable for low voltage operation.In S2CFF, the retentive problem of internal nodes is solved so that the FF can work correctly at low supply voltage. The main drawback of S2CFF is the waste of power consumption in redundant pre-charge and discharge operations.

Once the data input stays at logic low level, throughout the negative half cycle of CK, the node N2 pre-charges to VDD through M7 and discharges to GND via M8 and M10 at the positive edge of CK. Since output state is not impacted by the pre-charge and discharge phases and the node

capacitance seen on the node of n2 is huge it is observed that there is unnecessary wastage of power.

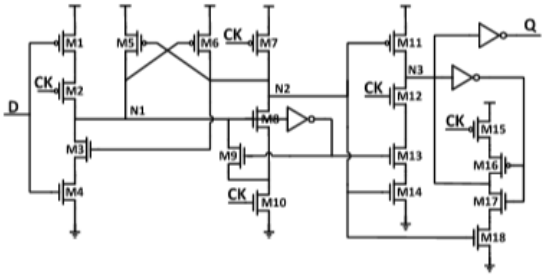

Fig.3 : Traditional S2CFF Flip-Flop.

To eliminate the energy-wasted operation, the pre-charge path should be cutoff when D = 0. A PMOS M1 controlled by the inversion of the input data is inserted into the pre-charge path of the FF as shown in Fig. 4. When the input data is 1, the PMOS M1 is ON and the necessary pre-charge operation works as usual. When the input data remains 0, the PMOS M1 is OFF and the pre-charge path is cutoff by the inserted transistor. As a result, the redundant pre-charge operation is totally removed.

The block diagram of the Flip-Flop by eliminating the pre-charge scheme is shown below.

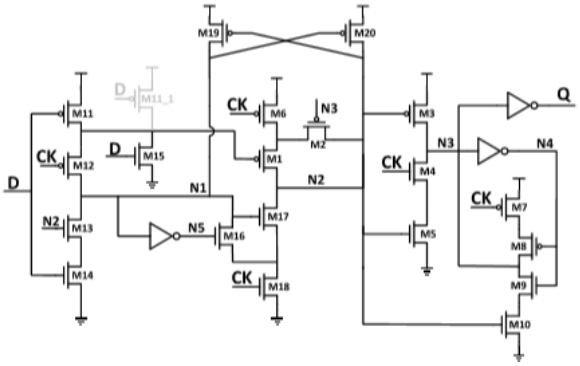

Fig.4 : True single phase clock based Flip-Flop

In digital systems, FFs usually need to have additional functions such as set, reset, and scan. These extra functionalities can simply be added to the FF that has been suggested. Figure 5 shows a schematic of the proposed FF with these additional features.

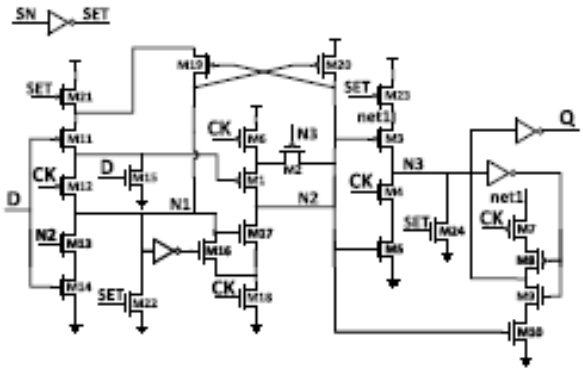

Fig.5: TSPC Flip-Flop with set

As shown in Fig. 5, when the set signal SN is low, SET is high, the charging path of N1 is cutoff by M21, and N1 is pulled down through M22. Since the node N1 is low, N2 is charged to VDD through M20. At the same time, the charging path of N3 is cutoff by M23, N3 is pulled down through M24, and the output keeps high.

Show the Fig 6 schematic of the proposed FF with reset function. As shown in Fig.6, when the reset signal RSTN is low, RST is high, the charging path of N2 is cutoff by M21, and N2 is pulled down through M22. Since N2 is low, N3 is charged to high through M3, and the output Q keeps low. At the same time, N1 is charged to high through M19. A PMOS M23 is inserted to isolate N1 from the input to avoid short circuit current through M12 and M15 when CK=0 and D =1.

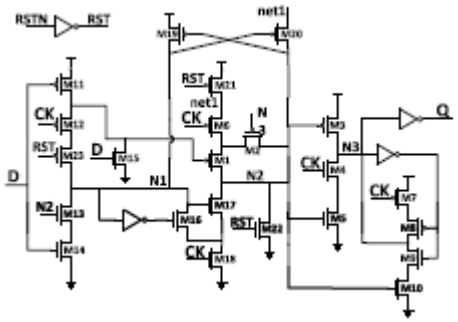

Fig. 6 : Schematic of proposed Flip-Flop with reset.

Fig. 7 shows the schematic of the proposed FF with the scan function .The input data D is detached from the FF when the scan enable signal SE is made high, and the FF records the scan input SI data at the

positive edge of CK, as illustrated in Fig. 7. When SE is logic low, SI is separated from the FF, and at the rising edge of CK, the FF collects the input data D.

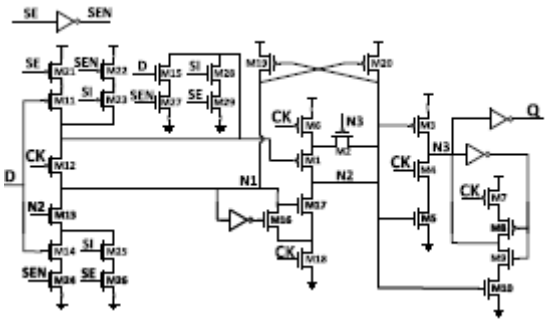

Fig.7 Schematic of TSPC Flip-Flop with scan input.

As the technology has been scaling down in the recent years, along with the technology, the supply voltage is also being scaled due to which the soft error effect has become the major concern. The schematic of proposed soft error tolerant Flip-Flop is shown below.

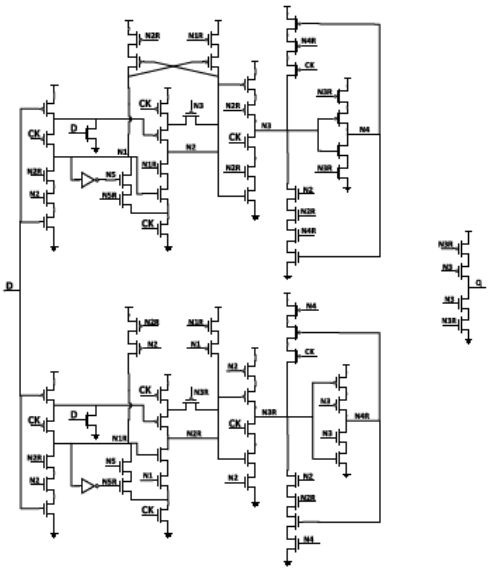

Fig.8 : Schematic of TSPC based soft error tolerant Flip-Flop

III. IMPLEMENTATION

Continuous scaling of process technologies enhances chip performance and density, enabling for more computations to be performed in a smaller space. However, as technology advances, electricity usage rises dramatically. Today's electronic devices, such as mobile phones and laptop computers, must have a high battery life. Heat is generated by power usage, necessitating the installation of costly cooling systems in servers and modern computer equipment. All of these reasons have forced designers to concentrate on low-power digital circuit design approaches.

Power consumption in digital circuits may be divided into two categories termed as dynamic and static. [3, 5]. Dynamic power dissipation is caused by the charging and discharging of transistor and wire capacitance. Technology scaling demands decreasing the supply voltage to prevent transistor breakage owing to excessive electric fields. Supply voltage scaling also saves a significant amount of dynamic power, albeit at the cost of performance. To maintain performance, the thresh-old voltage should be adjusted [6]. On the other side, lowering the threshold voltage causes higher leakage. Because the connection between threshold voltage and leakage is exponential, leakage power, also known as static power, is becoming a greater percentage of overall power consumption.

Flip-Flops are the basic Memory elements in many applications such as registers, counters which are mainly used in portable application. Hence low power consumption is need of the day. Due to technology scaling, the Leakage power consumption is the major concern. To overcome this leakage problem, in this method, header power gating technique is implemented in the proposed TSPC Flip-Flop. By applying this power gating technique to the Flip-Flop the power consumption is reduced since we are shutting down the power supply when not required.

Sub threshold leakage currents will become an increasingly major component of total power dissipation as future technologies scale and reduce power consumption. One of its most successful leakage power reduction approaches is power gating.

In this paper, we offer a power gating technique for D-Flip-Flop to minimize the power dissipation.

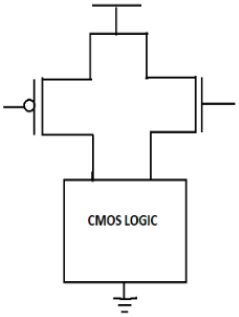

Fig.9: Block diagram of Power Gating

It can be observed from the fig.6 that when the gates of both pmos and nmos are on only the supply will be passed to the circuit. The circuit diagram of power gated TSPC Flip-Flop is shown in Fig.10.

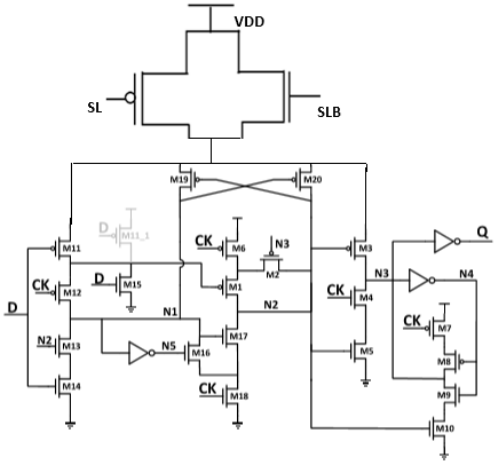

Fig.10: Proposed power gated TSPC Flip-Flop.

IV. RESULTS AND DISCUSSION

The schematic diagram and waveform of power gated TSPC based Flip-Flop is shown in Fig.11 and Fig.12 respectively. Simulations are performed with the help of Tanner EDA tool using 45nm technology.

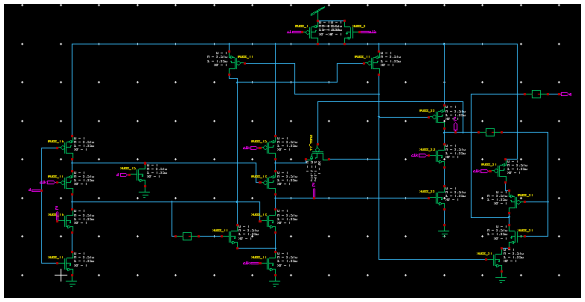

Fig.11: Schematic diagram of TSPC Flip-flop

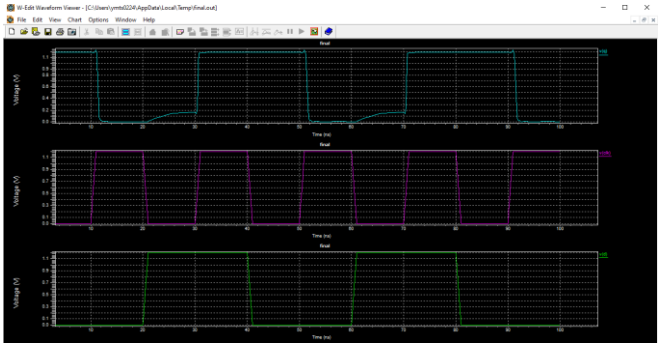

Fig.12: Waveform of proposed D Flip-flop

In Fig 12 the input is D, clock and output is Q By removing the redundant pre charge and discharge operation the power of the proposed D flip flop is greatly reduced and it will avoid the generation of the short circuit. One of the most generally used methods for decreasing consumption is power gating, which involves turning off the connection to the power source while it is not in use. The proposed flip-flop design uses the power gating principle to reduce power usage by only passing power to the circuit when it is needed.

Table 3: Comparison of Existing and Proposed work

	Power(uw)	Delay(ns)	Area
Existing FlipFlop	209	0.7	28
Proposed FlipFlop	157	0.7	19

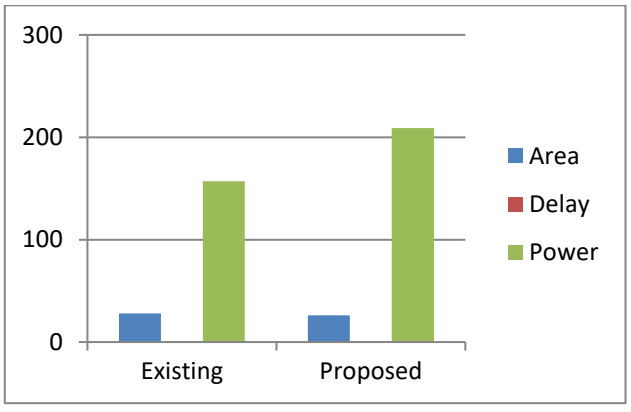

Fig.13 Comparison of area between existing and proposed method

V. CONCLUSION

The design of power gated true single phase clocked (TSPC) Flip-Flop is presented in this article. Power gating is one of most widely technique for reducing consumption by shutting down the connection from the supply when not required. By applying the power gating concept, power consumption is minimized in the proposed flip-flop design since the supply is passed to the circuit only when required in the proposed D Flip-Flop design Existing Flip-Flop power is 209uw and Proposed FlipFlop power is 157uw

VI. REFERENCES

[1]. F. Chang et al., Practical Strategies for Power-Efficient Computing Technologies, Proceedings of the IEEE, Vol. 98, No. 2, pp. 215-236, 2010.

[2]. R. N. Agnes Shiny, B. Fahimunnisha, S. Akilandeswari and S. J. Venula, Integration of Clock Gating and Power Gating in Digital Circuits,2019 5th International Conference on Advanced Computing & Communication Systems (ICACCS), 2019, pp. 704-707.

[3]. S. M. Sharroush, Impact of technology scaling on the performance of DRAMs, 2016 5th International Conference on Electronic Devices, Systems and Applications (ICEDSA), 2016, pp. 1-4

[4]. M. Aguirre-Hernandez and M. Linares-Aranda, A Clock-Gated Pulse-Triggered D Flip-Flop for Low-Power High-Performance VLSI Synchronous Systems, 2006 International Caribbean Conference on Devices, Circuits and Systems, 2006, pp. 293-297.

[5]. B. Aparna and V. Anandi, Design of a D flip flop for optimization of power dissipation using GDI technique,2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), 2017, pp. 172-177.

[6]. N. Nedovic, M. Aleksic, and V. G. Oklobdzija, Conditional techniques for small power consumption flip-flops, in Proc. 8th IEEE Int. Conf. Electronics, Circuits Systems, Malta, Spain, Sept. 2–5, 2001, pp. 803–80.

[7]. Bonetti, A. Teman and A. Burg, An overlap-contention free true-single-phase clock dual edge triggered flip-flop, Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), pp. 1850-1853, May 2015.

Cite this article as :

Triveni Jagadi, Vilaskumar Patil, "Implementation of TSPC Flip-flop using Power Gating Technique", International Journal of Scientific Research in Science and Technology (IJSRST), Online ISSN : 2395-602X, Print ISSN : 2395-6011, Volume 9 Issue 4, pp. 361-366, July-August 2022.

Journal URL : https://ijsrst.com/IJSRST229452