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# Power Efficient and Modified Transmission Technology Based Sram Cell for Core Memories

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**ABSTRACT**

The suggested circuit in this project is designed for IoT applications employing a modified transmission gate based SRAM cell that eliminates the need for peripheral circuitry during read operations. Biomedical systems that operate in the sub-threshold region with near-perfect efficiency require several kB of embedded memory. SRAMs account for 70% of the die area, which means they consume the most power and consume the most silicon. In the read operation, this topology provides a smaller area, less delay, lower power consumption, and better data stability. The SRAM cell is made of 45nm CMOS and runs at 0.45 V.
Keywords : SRAM, IOT applications, Low power, power gating.

## I. INTRODUCTION

The development of a low-power Static Random Access Memory (SRAM) is important for implantable devices and wireless applications where input power or battery life are important [1], [2], and whose operational frequency spans from a few hundreds of Kilohertz to tens of Megahertz [3]. This is due to the SRAMs' significant contribution to System on Chips (SoCs), as they occupy roughly 70% of the die space, which could be expanded in the future [4]. SRAMs have become increasingly power hungry as the number of transistors has increased and the leaking current of these transistors has decreased in scaled down technologies.

In core memory, power consumption is a crucial factor. As a result, we are employing several power reduction approaches in order to minimize the overall circuit's power consumption while also improving its overall performance. Power gating technique, adiabatic, clock gating, GDI, and lector approach are some power strategies that can be used to lower a circuit's average power use to reduce the average amount of energy used We used the power gating strategy in our project's supply voltage as part of the proposed design. Static random access memory's performance, size, and power consumption has a big impact digital integrated systems. Low-power circuits that can function for the aforementioned implanted and wireless applications, long-lasting devices that take up less space without sacrificing performance are necessary, as this is inconvenient and possibly dangerous, especially in the case of implantable devices.

Because the leakage because supply voltage has an exponential and quadratic relationship with power

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and active power, reducing the supply voltage is one of the most straightforward and cost-effective methods of increasing energy efficiency [5]. Alternatively, lowering the supply voltage can help, would reduce the circuit's robustness and could wreak havoc on the system As a result, decreasing the supply voltage while maintaining circuit robustness is crucial for power-constrained devices, because data integrity is one of the SRAM cells' core concerns.

As a result of the loss of write ability and read consistency in the near and sub-threshold area, the conventional 6T cell ceases to function [6]. It is preferable to utilize a broad access transistor for a successful write operation, but this may have an impact on read stability. This is a compromise between data stability and write and read performance. Researchers proposed a number of cells based on eliminating the read/write stability tradeoff. These concepts, such as [7] cells, rely on decoupling the read port from the write port by splitting the read and write routes, allowing each process to be improved separately.

They are, however, susceptible to leakage current, need a wide area, or use an approach that minimizes read sensitivity by using a read with only one ending [17] To avoid the drawbacks of a single-ended read approach, numerous techniques [5] have been applied, such as increasing the differential read port by adding extra transistors, albeit at the cost of additional space. Another method devised to improve stability was the use of transmission gates. This brief offers a new 8T SRAM cell based on Transmission gates that is specifically intended for Read operation and enhances Read Noise Margin while consuming less power and time.

It saves space by using fewer transistors and eliminating read-only peripheral circuitry. The following is how the rest of the document is structured: Section-II discusses the fundamental architecture of static random access memory (SRAM), Section-III simulates the operation of standard 6T, 8T, and other existing 10T SRAM cells, and Section-IV describes the proposed SRAM's performance 8T SRAM cell in detail, Section-V compares the proposed cell to the existing ones, and Section-VI concludes the presentation. A block diagram of a typical SRAM design is shown in Figure 1 [19]. Memory Array, Row Decoder, Column Decoder, Precharge circuit, and Sense Amplifier are the most important components of the SRAM chip.

Data will be saved or read in the memory array, which is made up of a number of cells. A single piece of data can be stored in each cell. A row decoder and a column decoder are used to select a specific cell from an array. Bit Lines are pre-charged is started via the precharge circuit. The read function is handled by a Sense amplifier in particular. It detects a cell's content as a slight voltage change between the cell's Bit Lines and generates the data that is stored in that cell.

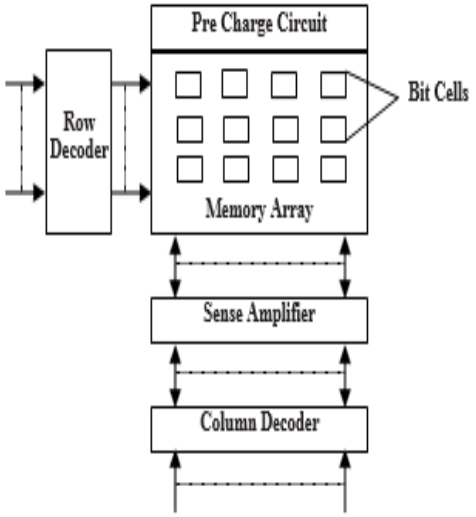


Fig1: Architecture of SRAM

Memory cells are a fundamental component of SRAMs because they take up a large amount of space. The 6T SRAM cell is easy to implement, Figure 2 illustrates this. The cell is made up of two cross-coupled inverters and two pass transistors. The fundamental latch is provided by the two cross-coupled inverters, which can store one bit of data. The two Pass transistors are wired together in a circuit outside world via two complimentary types a Word Line and two Bit Lines (BL and BL Bar) are two types of bit lines (WL).

The three most prevalent states of SRAMs are read, write, and hold. The Word Line is disabled for a Hold operation by disconnecting the link between the cell and the Bit Lines. While the two cross coupling inverters are linked to the power supply, the data will continue to be strengthened. In preparation for a Read operation, the voltages on the two Bit Lines are equalised, and the Word Line is asserted. Bit Lines are a type of data that can be used to create a variety of will now be discharged to the ground, while the other will remain at Vdd, based on the information stored on two nodes of storage For example, let's say the storage node Q has a value of '1' and the storage node QBar has a value of '0.'

The current flows from Vdd to BL via M1 and M5, and BLBar is dumped to ground by M6 and M4. As a result, the two Bit Lines are separated by a small voltage differential, with BL having a greater voltage level than BLBar. The Sense Amplifier receives this little voltage difference and identifies and amplifies the signal, producing the appropriate value on the storage node Q.

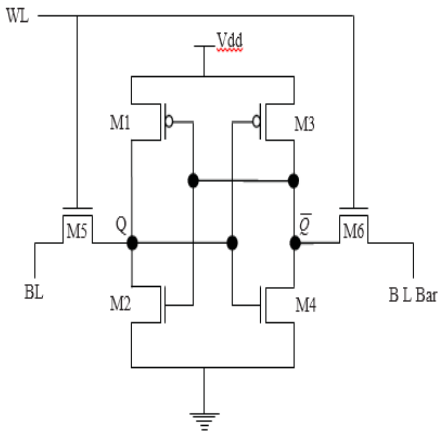


Fig2: 6T SRAM Cell (Traditional)

A conflict between the access transistors compromises the read stability of a traditional 6T SRAM cell and the pull down and pull up To address these challenges, a variety of cells have been developed, beginning with Figure 3 shows the 8T SRAM cell architecture [21]. The cell contains a decoupled read path with two extra nmos transistors to prevent read disturbance.

However, due to the additional transistors dependent on the information contained in the cell, it has a leakage problem. Complex peripheral circuitry, including as a For the traditional 6T, you'll need a precharge circuit, write drivers, and a sensing amplifier and more sophisticated devices listed in this section. The peripheral circuits that encircle the cell region take up a significant amount of space in the total macro cell.

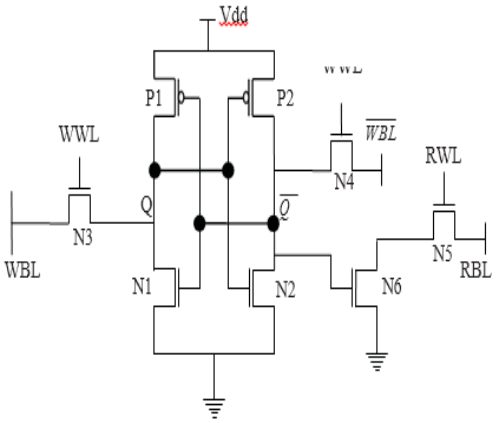


Fig 3:8T SRAM Cell

## II. EARLIER WORK

The design of a low-power Static Random Access Memory (SRAM) is important for implantable devices and wireless applications in which input power or battery life are important [1], [2], with operational frequencies ranging from a few hundreds of Kilohertz to tens of Megahertz [3]. This is due to the significant contribution of SRAMs on System on Chips (SoCs), which account for around 70% of the die area and could be enhanced in the future [4]. As SRAMs are becoming more and more power hungry, they have become more expensive.

The number of transistors has increased while leakage current has decreased in scaled-down technologies. Digital integrated systems' performance and power consumption are affected by their performance, size, and static random access memories. Low power circuits that can run for a long time are required for the implanted and wireless applications indicated above while taking up less space without deteriorating performance, as this is inconvenient and potentially

dangerous, especially when contemplating implantable devices.

Because the leakage power and active because power has an exponential and quadratic connection with supply voltage, reducing the supply voltage is one of the most simple and cost effective ways to improve power efficiency [5]. On the other side, lowering the supply voltage, would reduce the circuit's robustness and could resulting in the failure of the system As a result, decreasing the supply voltage while maintaining circuit robustness is crucial for power constrained devices, as data integrity is one of the SRAM cells' core concerns. Each bit is stored using bistable latching circuitry in a 6T static random-access memory. Static RAM is distinguished from dynamic RAM, which needs to be refreshed on a regular basis. SRAM may remember data, but it's still volatile in the traditional sense, meaning that when the memory is turned off, it's still there, data is lost.

SRAM ARCHITECTURE:

The primary components of the SRAM chip include the Memory Array, Row Decoder, Column Decoder, Precharge circuit, and Sense Amplifier. The memory array is made up of a number of cells that will be used to store and read data. One byte of data can be stored in each cell. To choose an individual cell from a group of cells, a row decoder and a column decoder are employed. Precharging of Bit Lines is started via the precharge circuit. The read function is handled by a Sense amplifier in particular. It detects a cell's content as a slight voltage change between the cell's Bit Lines and generates the data that is stored in that cell.

OPERATION OF A 6T SRAM CELL:

1. Standby Mode (the circuit is idle):

Because the word line is not asserted in the 6t cell's pass transistors N3 and N4, which connect the word line to the bit lines, are in standby state (word line=0), are deactivated. The cell can't be contacted, as shown by this message. While As long as two cross coupled inverters are fed back to each other, they will continue to feed back to each other N1-N2 are linked to the supply, the data will be retained in the latch. 2. Read Mode (the data has been requested):

In read mode, the word line is asserted (word line=1). The word line enables the access transistor as well as the bit line connector. The nodes' values are now passed. To the bit lines (nodes a and b). Assume that node a store's 1; the bit line bar will discharge through the driver transistor as a result (N1), and the bit line will be disconnected be pulled up toward VDD through the Load transistors (P1), resulting in a logical 1. Read stability is required in the design of SRAM cells (do not disturb data when reading).

Write Mode (updating the contents) Assume the cell was originally set to store a 1 and that we want to change it to a 0. To do so, lower the bit line to 0V and raise the bit bar to VDD, then raise to choose a cell, change the word line to VDD. Because each inverter is built with PMOS and NMOS matching, the inverter threshold is frequently set to VDD/2. If we want to write 0 at node a, N3 will be saturated. At initially, the source voltage is set to one. N2's drain terminal is originally at 1, which is driven down by N3 since access transistor N3 is stronger than N1. Now that N2 is on and P1 is off, a new value is written, causing the bit line to be lowered to 0V and the bit bar to be set to VDD. To work in write mode, SRAM must have write ability, the minimum bit line voltage necessary to flip a cell's state is defined as.

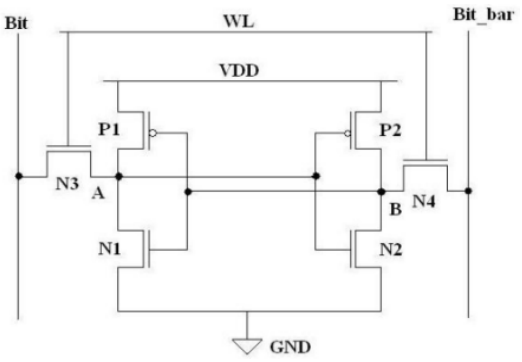


Fig4: Schematic of 6T SRAM Cell

Because of the decrease of write ability and read stability in the near and sub-threshold area, the conventional 6T cell ceases to function [6]. It is preferable to utilise a broad access transistor for a

successful write operation, but this may have an impact on read stability.

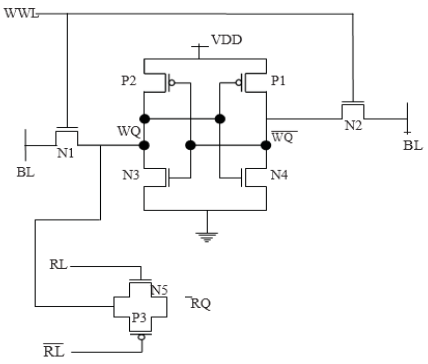


Fig5: 8T SRAM

The read operation is the main focus of the 8T SRAM design, whereas in prior systems, the read operation was limited to peripheral circuits. The Write process is identical in Conventional and other SRAM cells. Writing functions are handled by the Word Line (WWL). The Bit Lines BL and BL Bar receive the content that we want to write. The data from the Bit Lines can now intrude into the memory cell thanks to the enabled Word Line activating the access transistors. Intruded data will be cached in the WQ and WQBar storage nodes. The two complementing Read Lines RL and RLBar regulate the read operation, and they must both be enabled before the read can begin. By using a Transmission gate, the read port is created individually.

## III. PROPOSED WORK

The design of a lowpower Static Random Access Memory (SRAM) is important for implantable devices and wireless applications where input power or battery life are important [1], [2], and whose operational frequency spans from a few hundreds of Kilohertz to tens of Megahertz [3] This is owing to SRAMs' substantial contribution to System on Chips (SoCs), since they account for around 70% of die area, which could be enlarged in the future [4]. As the number of SRAMs has grown, they have become more power hungry.

Transistors has increased and the leaking current of these transistors has decreased in scaled down technologies. Many different cells have been constructed in order to tackle the leakage problem. In [22], a circuit known as 10T-E1 was proposed as a recent work. A pmos transistor is included in the read path, which reduces the leaking current through the M6 transistor. However, the design also causes leaky current to pass from the node to the RBL, lowering the sensing margin and making the system data-dependent.

Modifies 10T-E1 by constructing Figures 5 and 6 show SRAM cells with only NMOS read ports (Referred as 10T-E2 and 10T-E3). The reading function is handled by a separate read port made up of four NMOS transistors (R1, R2, R3, and R4). Both designs contain isolated read ports, resulting in a more stable and less destructive read operation. Because the separate read port employs a transistor stack, bit line leakage is reduced.

The existing 10T cell, as well as many other comparable cells, improve read stability at the cost of increased space because they require a greater number of transistors. However, in many applications, such as biomedical and wireless, area occupancy is crucial. When it comes to biomedical implants, less device area occupancy inside the body means less intrusion into the human body. This brief proposes an 8T Transmission gate based SRAM cell in response to such a design challenge with SRAMs. By reducing peripheral circuitry, this design decreases the amount of space needed. Complex peripheral circuitry, including as a For the traditional 6T, you'll need a precharge circuit, write drivers, and a sensing amplifier and more sophisticated devices listed in this section. The peripheral circuits that encircle the cell region take up a significant amount of space in the total macro cell. According to a recent statement [25], the peripheral circuitry should account for roughly 25% of the macro area.

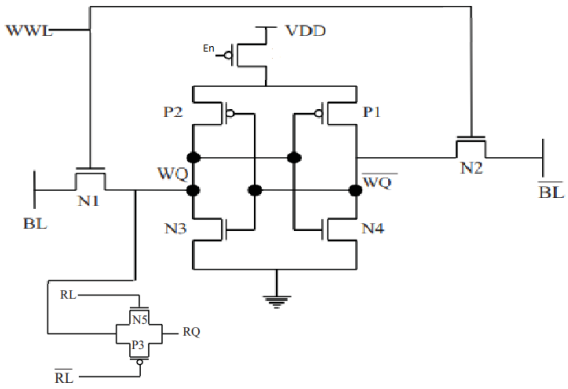


Fig6: proposed modified transmission gate based sram cell

The suggested modified transmission gate based SRAM cell focuses primarily on the read operation, which is now carried out solely by peripheral circuits in conventional designs. The Conventional and other SRAM cells have the same Write operation.

Writing functions are handled based on the word line (WWL). The Bit Lines BL and BL Bar receive the content that we want to write. The data from the Bit Lines can now intrude into the memory cell thanks to the enabled Word Line activating the access transistors. Intruded data will be cached in the WQ and WQBar storage nodes. The two complementing the read operation is governed by Read Lines RL and RLBar, both of which must be enabled before the read can commence.

The read port is protected by a transmission gate created individually. The main goal here is to read data from the WQ storage node. As a result, the data cached in the storage node WQ is sent on to the Transmission gates N5 and P3, which are both turned on because the Read Lines have been enabled. The data is now passed to the Read node RQ through the Transmission gate. Through the data saved in node WQ will appear at node RQ, thanks to the N5 and P3 transistors.

The content of the cell can be programmed without the requirement for complex peripheral circuitry read directly using a Transmission gate. The following is the generalized read energy equation: Where VRBL is the read bitline voltage, and V1 is the read bit line voltage once the read operation is completed. The read energy can be lowered with this design because the sense amplifier and precharge circuit are not used. This design decreases a 15 percent reduction in the number of transistors required to construct peripheral circuits, resulting in a 15 percent reduction in chip area the total quantity of power consumed drops as the number of transistors used lowers. This is because, as we'll see later, the number of transistors used in a design affects the leakage power.

$$P_{total} = P_{dyn} + P_{Leak}$$

$$P_{dyn} = CeV^2 \ f$$

$$P_{Leak} = Vdd \ Ntr \ Kd \ Is$$

Ntr signifies the number of transistors, Kd the device-specific constant, and I the normalised static current for each transistor. The lower the transistor count, the lower the leakage power of the transistors, and thus the lower the overall power dissipation of the circuit. The latency of creating the output, i.e. because the sense amplifier and precharge circuits used for read functionality in conventional designs are deleted in the suggested design, the time it takes to read the data stored in the storage nodes can be lowered as well. As a result, the read operation is carried out quickly with the help of the transmission gate.

This method also provides stability because the read and write ports are separated. A transmission gate's averaging effect two parallelly positioned transistors helps to neutralise the read current, resulting in superior stability than when the read current passes through a single NMOS transistor. By assuming the cell failure probability can be calculated using the Gaussian Distribution for a transistor's Threshold voltage [26] estimated. The formula is as follows:

$$P_{fail} = Prob$$

$$[SNM < V_{th}]$$

$$Where, \ V_{th} = kT/q$$

$$kT = 26 \ mV \ at \ 300K$$

Because the design is solely designed to perform the read process, the comparison of the suggested design is done for the read operation itself. The performance

findings are also homogeneous, as the Write and Hold actions are similar to the previous designs.

As a result, in the study offered here, the read status is taken into account. Power consumption, latency, stability, and cell area occupancy are common measures used to assess SRAM performance. The team's performance Conventional 6T (C6T), several current approaches (8T, 10T-E1, 10T-E2, and 10T-E3), and the Proposed 6T (P6T) in CMOS 45-nm Technology at 0.45V at room temperature methodology (8T-P) are compared.

## IV. EXPERIMENTAL RESULTS

The comparison of the proposed design is done for the read operation itself since the design is intended to perform the read process only. Since the Write and Hold operations are similar to the existing designs, the performance results are also homogeneous. Therefore the results discussed here considers the read state. Generally, the performance analysis of SRAMs is based on certain parameters such as Power Consumption, Delay, and Stability and Area occupancy of the cell. The performance comparison of the Conventional 6T (C6T), other existing techniques (8T, 10T-E1, 10T-E2 and 10T-E3, 8T-P) and the Proposed power gating technique based modified 8T transmission gate is done in CMOS 45-nm Technology at 0.45V at room temperature.

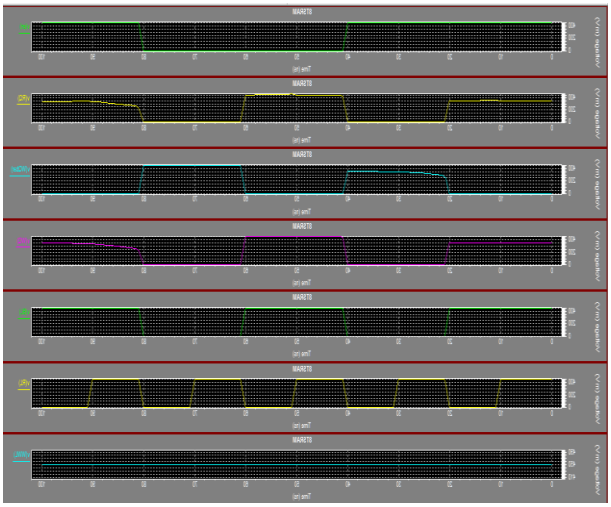

Fig 7: output simulation results of proposed SRAM

## V. CONCLUSION

Transmission with a change For IoT applications, a gate-based SRAM design was used. The read action is not required in this configuration because the read port is decoupled. Power consumption, latency, stability, and area are all improved as a result of such a design. Furthermore, the reduced transistor count can cut power usage by up to 99 percent when compared to conventional 6T and other ways. When compared to the conventional 6T, 8T, 10TE1, 10T-E2, and 10T-E3, eliminating peripheral circuitry during the read operation and doing it directly with transmission gates results in a latency optimization. When the cell stores 'zero' and 'one,' the suggested cell uses the least amount of power compared to conventional 6T, 8T, 10TE1, 10T-E2, and 10T-E3 cells.

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